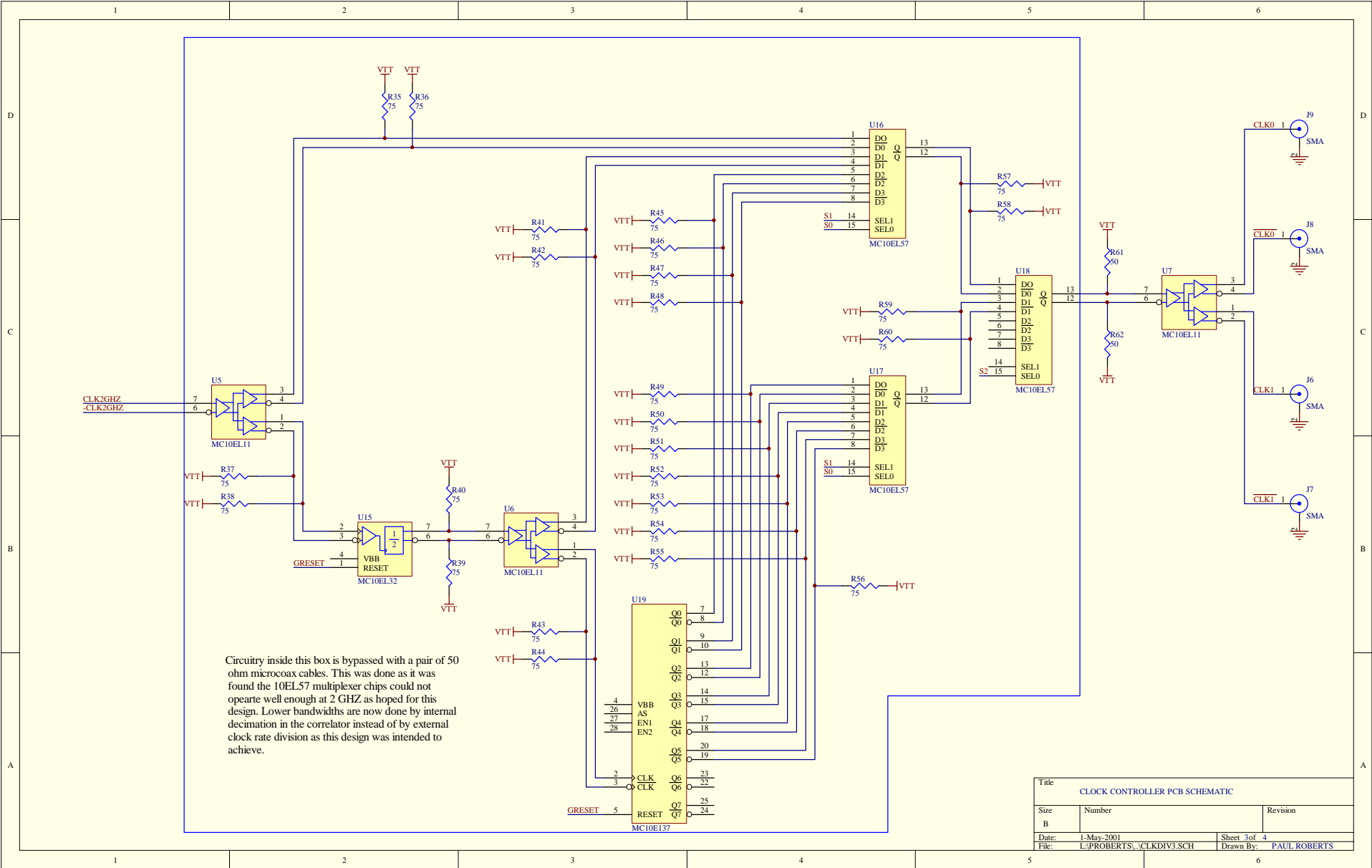


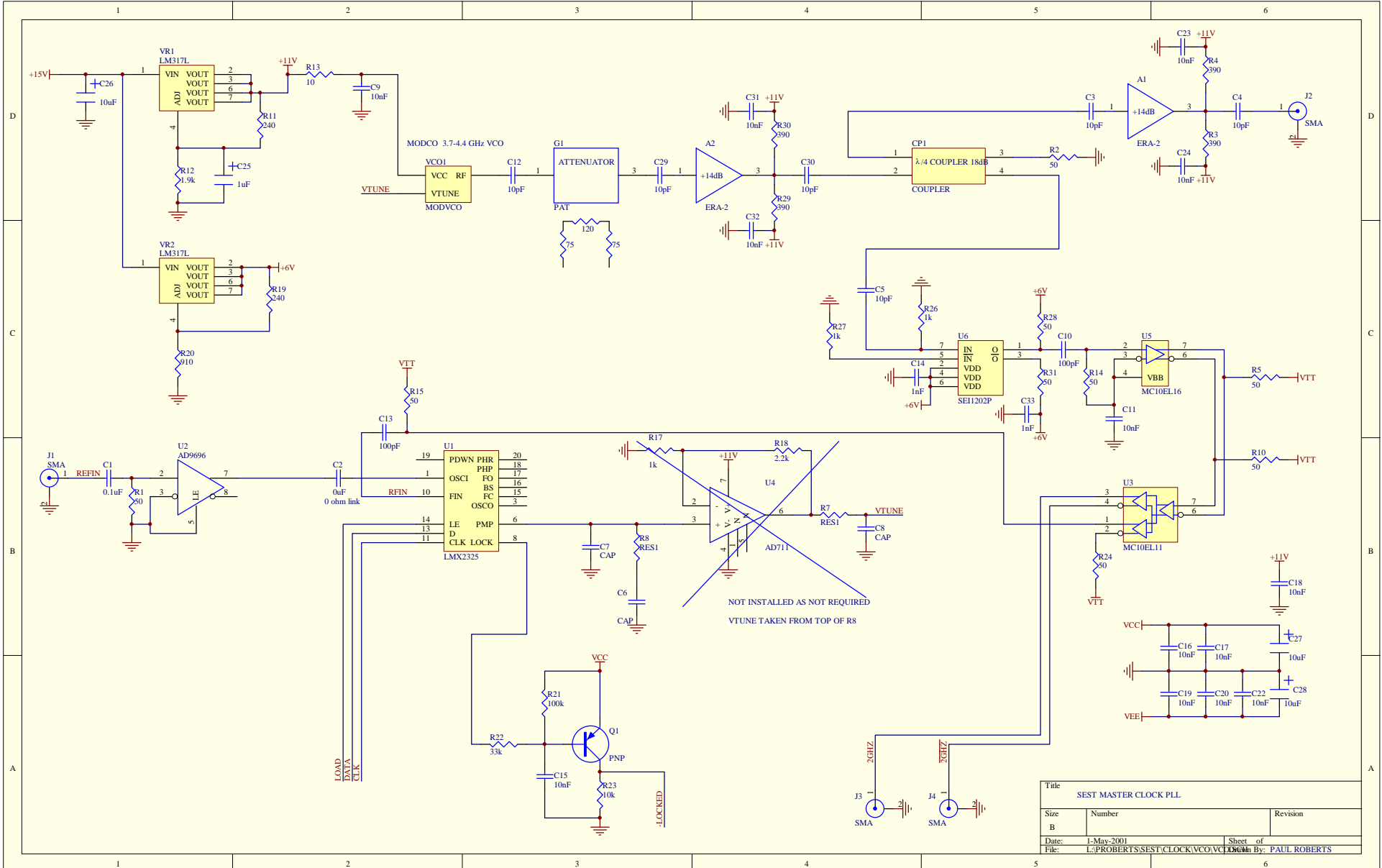
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CLOCK CONTROLLER PCB SCHEMATIC		
Size	Number	Revision
B		
Date:	1-May-2001	Sheet 2 of 4
File:	E:\PROBERTS\...CLKDIV2.SCH	Drawn By: PAUL ROBERTS



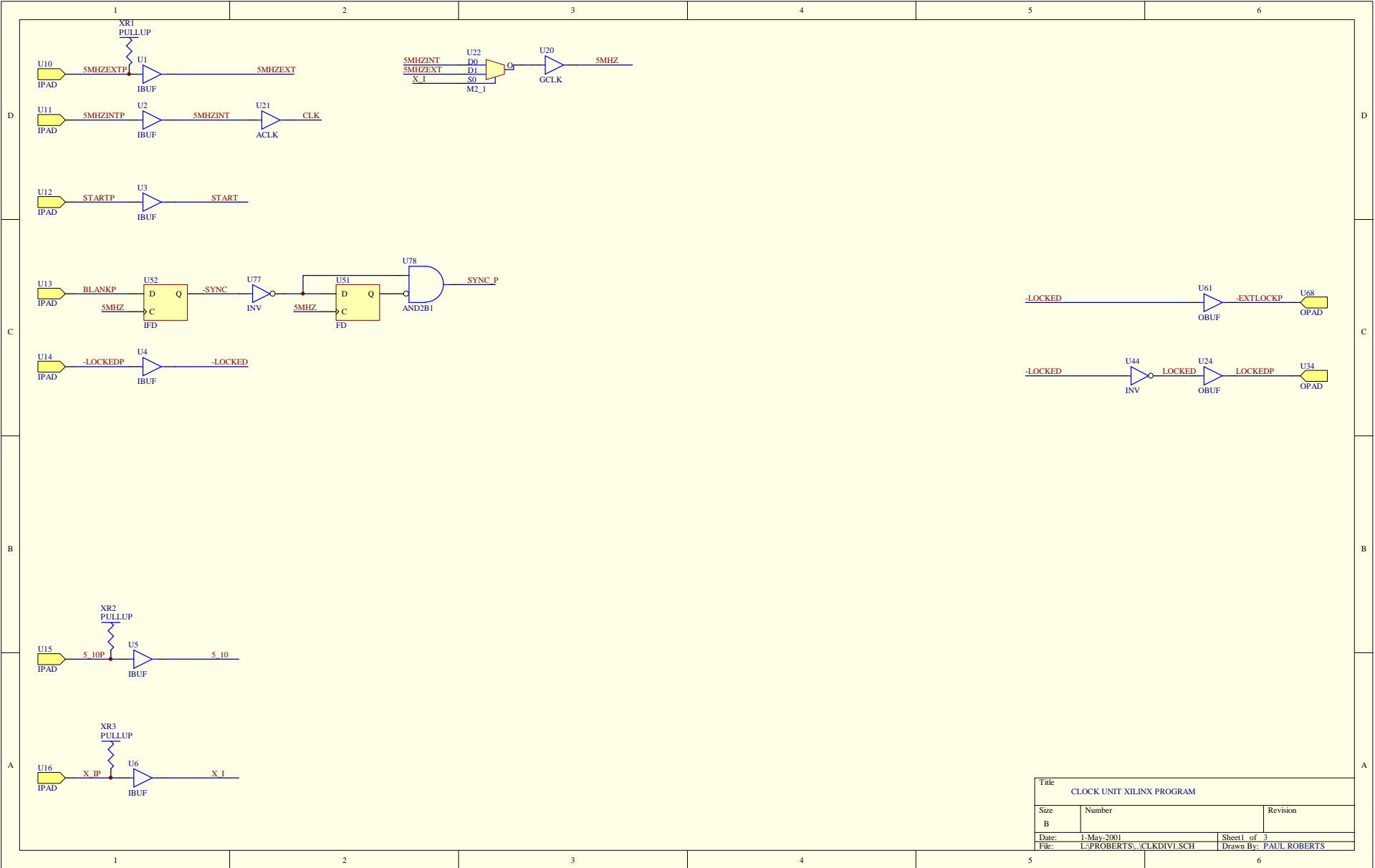
Circuitry inside this box is bypassed with a pair of 50 ohm microcoax cables. This was done as it was found the 10EL57 multiplexer chips could not operate well enough at 2 GHz as hoped for this design. Lower bandwidths are now done by internal decimation in the correlator instead of by external clock rate division as this design was intended to achieve.



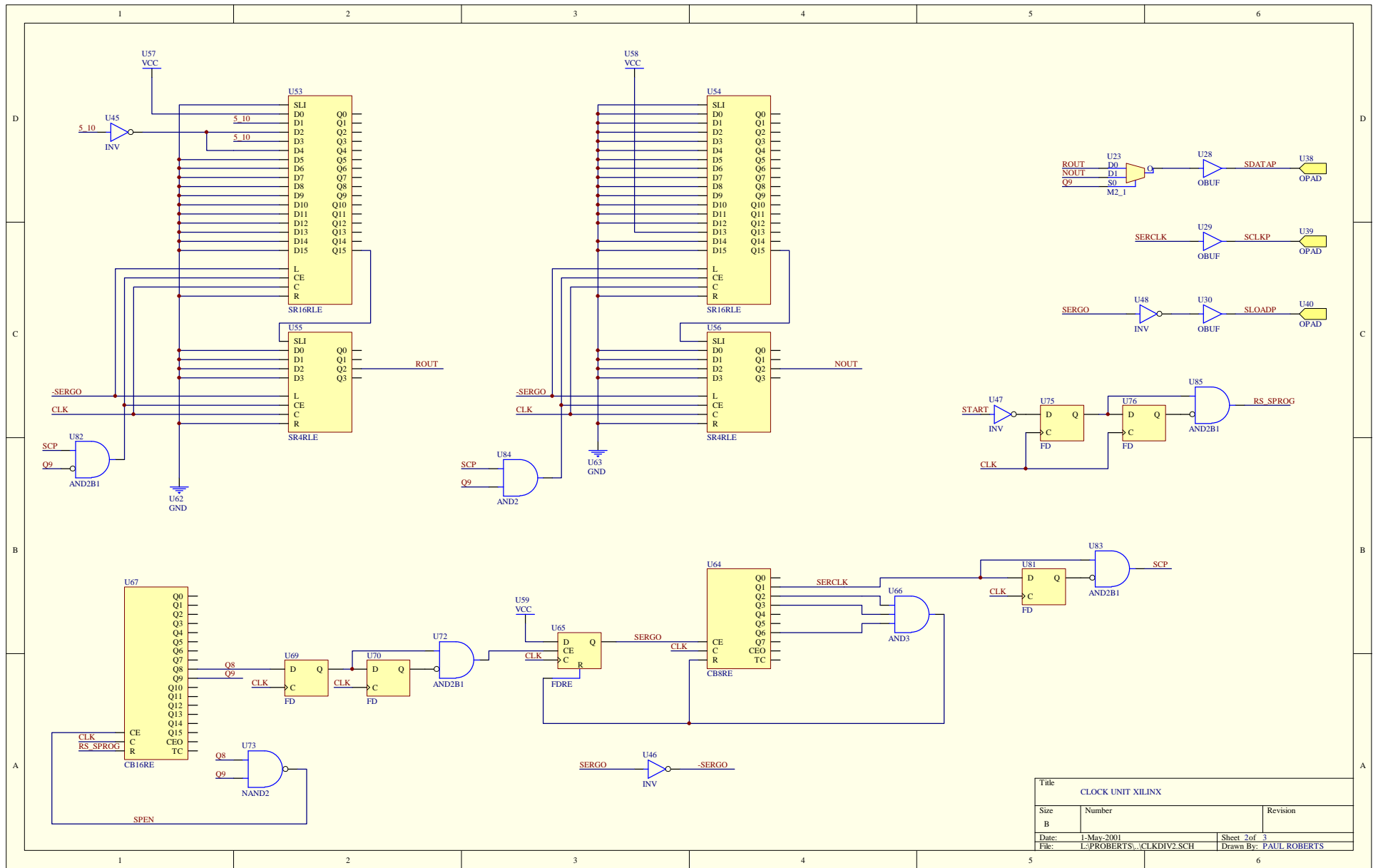
Title		
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Size	Number	Revision
B		
Date:	1-May-2001	Sheet 4 of 4
File:	E:\PROBERTS\...CLKDIV4.SCH	Drawn By: PAUL ROBERTS



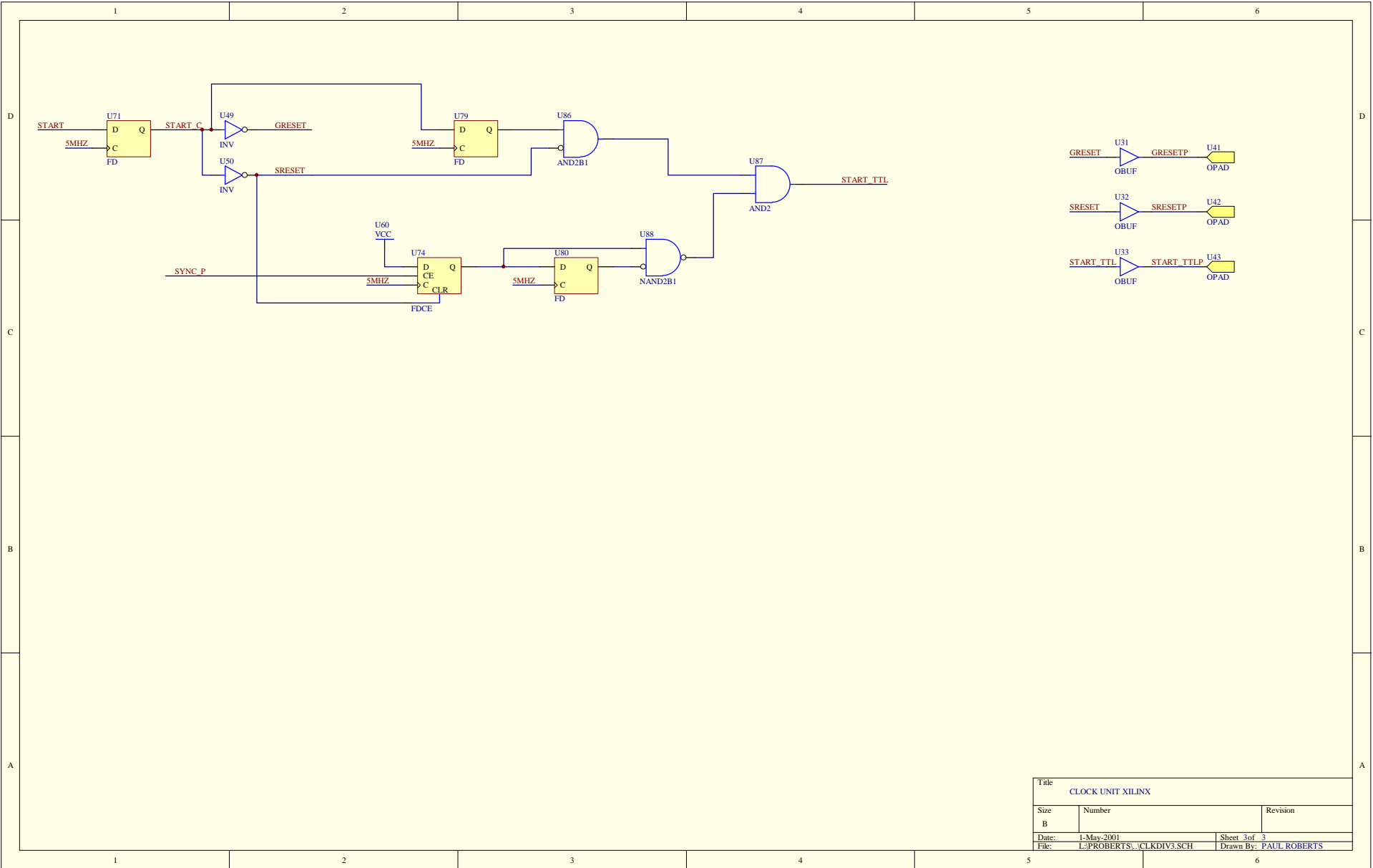
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SEST MASTER CLOCK PLL		
Size	Number	Revision
B		
Date:	1-May-2001	Sheet of
File:	E:\PROBERTS\SEST\CLOCK\VCO\VCLOCK.Dwg	Drawn By: PAUL ROBERTS



Title		
CLOCK UNIT XILINX PROGRAM		
Size	Number	Revision
B		
Date:	1-May-2001	Sheet 1 of 3
File:	E:\PROBERTS\...CLKDIV1.SCH	Drawn By: PAUL ROBERTS



Title: CLOCK UNIT XILINX		
Size	Number	Revision
B		
Date:	1-May-2001	Sheet 2 of 3
File:	E:\PROBERTS\...CLKDIV2.SCH	Drawn By: PAUL ROBERTS



Title		
CLOCK UNIT XILINX		
Size	Number	Revision
B		
Date:	1-May-2001	Sheet 3 of 3
File:	E:\PROBERTS\...CLKDIV3.SCH	Drawn By: PAUL ROBERTS



