Australia Telescope National Facility

SEST SAMPLER

Preliminary

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1.0 Introduction

The ATNF SEST sampler is a wideband, two-bit, three-level sampler operating at up to 2.048 Giga-samples per second for use with the ATNF SEST correlator. The function of the sampler is to sample and digitise an input IF passband of up to 1.024 GHz bandwidth and convert the data into a format compatible with the ATNF SEST correlator. Another key function of the sampler is to maintain the digitising thresholds at the optimum value for a three-level correlator to maintain maximum signal to noise ratio.

2.0 Physical Desciption

The sampler is housed in a 17" x 2U rack case. Inputs to the sampler consist of:
1) The input IF at an rms power level of ~0dBm at all bandwidths entering on a single rear bulkhead SMA connector.
2) A differential ECL clock at the sample rate entering on two rear bulkhead SMA connectors.

Data output from the sampler is 16 sample wide, 32 pair balanced ECL, physically consisting of two 34 way cables with 16 data signals and one clock in each cable. The clock is at half the output data rate with rising and falling edges aligned with the output data. Physical connection with the sampler is via two 37 pin female D type connectors.

Communication with the sampler is via a standard ATNF Interface card (16 bit parallel multiplexed address/data bus) from the correlator block control computer. The interface connects to the sampler via a 26 pin female high density D type connector. In addition an RS-232 serial port is provided for auxillary communications or status display on a serial terminal. The serial port connects to the sampler via a 9 pin female D type connector.The is also an output display port which drives a front panel 2 line by 20 character alphanumeric display.

The sampler physically consists of four sections:

1) The high speed buffer amplifier/comparater. This consists of a wideband buffer amplifier followed by a power spitter and dual high-speed comparator integrated onto a high dielectric constant substrate with 1/4 inch copper base. This section is contained within its own RF tight enclosure with the output ECL data exiting via small diameter (0.9mm) semi-rigid coax. This section is mechanically fixed to the high speed ECL board.

2) The high speed ECL board. This board latches the data from the comparators at up to 2.048 GS/s and performs a 1:4 serial to parallel conversion of the sampled data.

3) The medium speed ECL board. This board takes the 4 sample wide data from the high speed ECL board at speeds up to 512 MS/s and performs a further 1:4 serial to parallel conversion of the sampled data to give a final 16 sample wide data output to the correlator. This board also counts the number of samples in the outer quantisation levels and passes this to the control board to allow automatic control of the sampler threshold levels. This board is designed to operate at up to 1.024 GS/s to allow for future upgrade to wider bandwidths.

4) The control board. This board uses the outputs of the ripple counters on the medium speed ECL board to determine the statistics of the sampled data and from this control the sampler threshold levels with a real time digital feedback loop. This board also implements the sampler external communication interface via a standard ATNF Interface port, RS-232 serial port and front panel alphanumeric display port. The funtionality of the board is provided by an on board DSP processor and high density FPGA.

The ampifier/comparator, high speed ECL board and medium speed ECL board are all contained within an RF tight enclosure for maximum RFI immunity. Connection to the control board is via a 26 pin high density female D type connector for the digital control signals and two semi-rigid coaxial lines for the sampler threshold levels.

3.0 Electrical Description

3.1 High Speed ECL Board

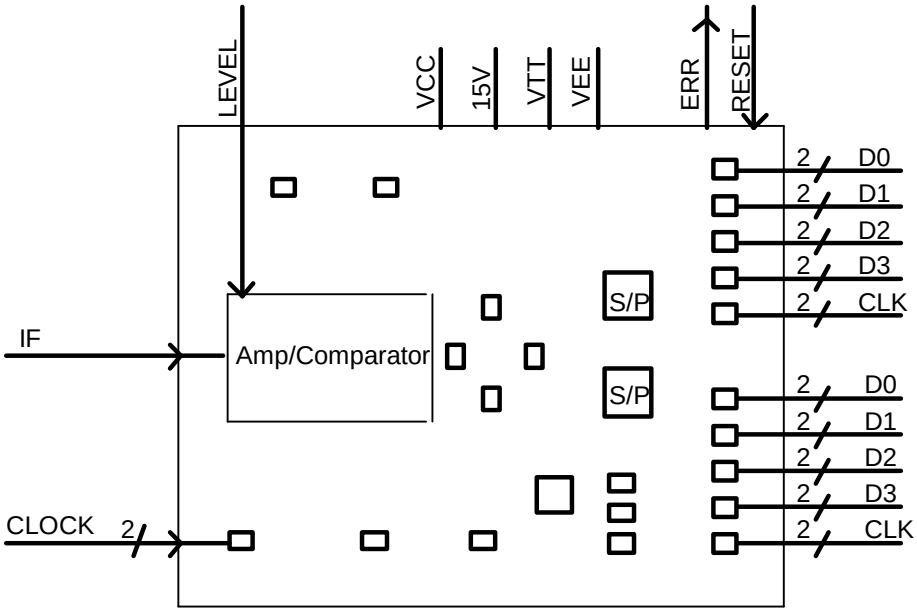


Figure 1. High Speed ECL Board

3.1.1 Signal Description

Signal	Type	Description
IF	Analogue @ 0 dBm	Analogue input
CLOCK	Differential ECL	Sample clock at up to 2.048 GHz
D0-3	Differential ECL	Output data. D0 oldest sample
CLK	Differential ECL	Data clock at the output data rate (i.e. CLOCK/4)
ERR	TTL	S/P converters out of sync error

RESET	10K ECL	Reset S/P converters and sync detection circuit

Table 1. High speed ECL board signal description

3.2 Medium Speed ECL Board

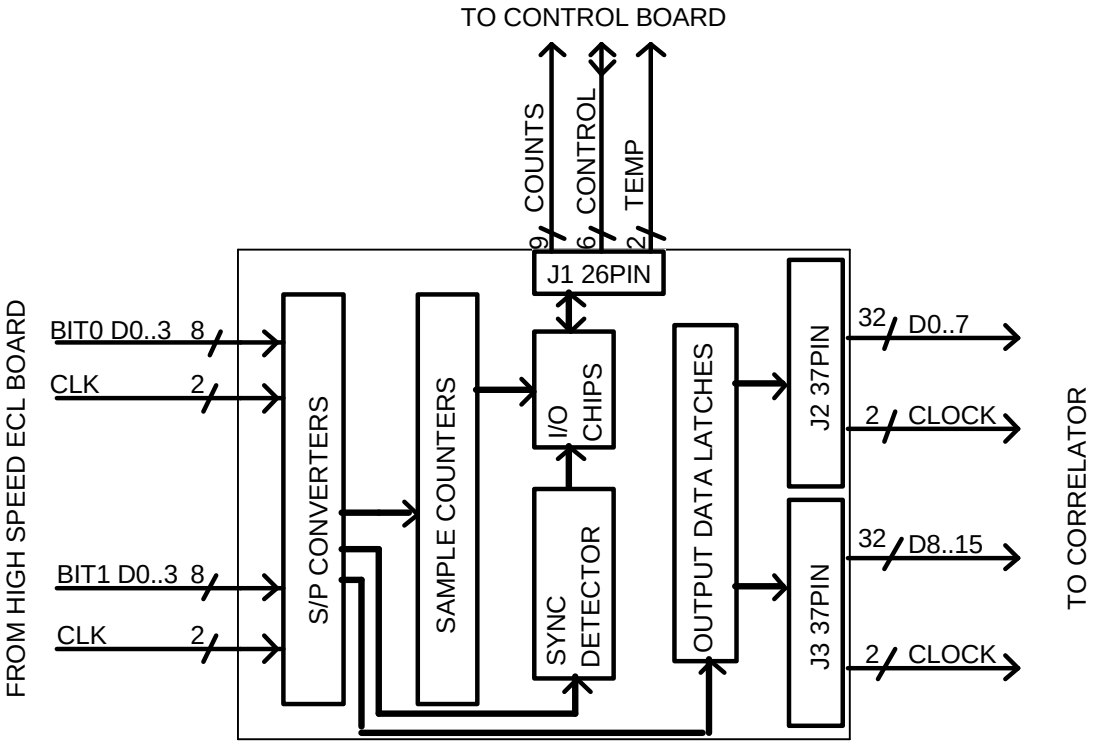


Figure 2. Medium speed ECL board

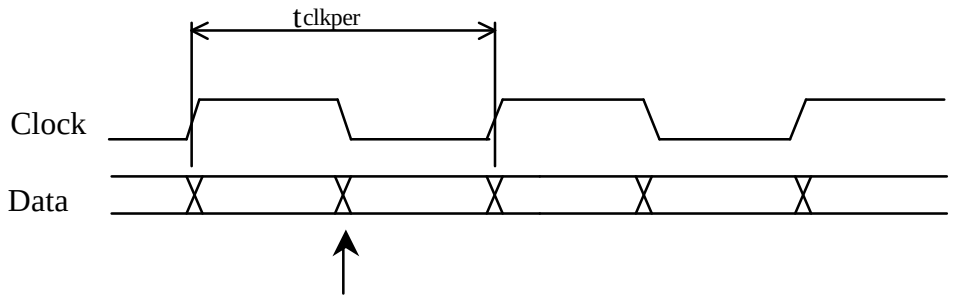
3.2.1 Signal Description

Connector J1

Pin	Type	Name	Function (All signals TTL levels)
1	O	COUNTA1	Sample counter D7 output
2	O	COUNTA2	Sample counter D7 output
3	O	COUNTA3	Sample counter D7 output
4	O	COUNTA4	Sample counter D7 output
5	O	COUNTB1	Sample counter D7 output
6	O	COUNTB2	Sample counter D7 output
7	O	COUNTB3	Sample counter D7 output
8	O	COUNTB4	Sample counter D7 output
9	O	CLKCOUNT	Clock counter D7 output
10	O	SYNCERR0	S/P converter Sync error on high speed ECL board
11	O	SYNCERR1	S/P converter Sync error on medium speed ECL board
12	I	GRESET0	Reset high speed ECL board
13	I	GRESET1	Reset medium speed ECL board
14	I	CRESET	Reset sample counters
15	I	CLENAB	Enable medium speed ECL board S/P converter clocks
16	I	TCLK	Temperature sensor data clock
17	I/O	TDATA	Temperature sensor serial data

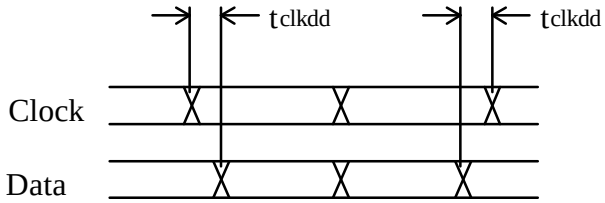
Table 2. Sampler-Correlator Cable Pin assignment.

	J1	J2
Wire	Signal	Signal
1	S0-D0	S8-D0
2	~S0-D0	~S8-D0
3	S0-D1	S8-D1
4	~S0-D1	~S8-D1
5	S1-D0	S9-D0
6	~S1-D0	~S9-D0
7	S1-D1	S9-D1
8	~S1-D1	~S9-D1
9	S2-D0	S10-D0
10	~S2-D0	~S10-D0
11	S2-D1	S10-D1
12	~S2-D1	~S10-D1
13	S3-D0	S11-D0
14	~S3-D0	~S11-D0
15	S3-D1	S11-D1
16	~S3-D1	~S11-D1
17	S4-D0	S12-D0
18	~S4-D0	~S12-D0
19	S4-D1	S12-D1
20	~S4-D1	~S12-D1
21	S5-D0	S13-D0
22	~S5-D0	~S13-D0
23	S5-D1	S13-D1
24	~S5-D1	~S13-D1
25	S6-D0	S14-D0
26	~S6-D0	~S14-D0
27	S6-D1	S14-D1
28	~S6-D1	~S14-D1
29	S7-D0	S15-D0
30	~S7-D0	~S15-D0
31	S7-D1	S15-D1
32	~S7-D1	~S15-D1
33	Clock	Clock
34	~Clock	~Clock



Data and Clock transition at the same instant.

SAMPLER-CORRELATOR DATA FORMAT



SAMPLER-CORRELATOR DATA-CLOCK TIMING

Name	Symbol	Min	Typ	Max	Units
Clock Period	tclkper	7.8	-	-	nS
Clock-Data delay	tclkdd	-0.25	0	0.25	nS

INFORMATION IN THIS DOCUMENT IS PRELIMINARY AS DESIGN IS STILL IN PROGRESS

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