The Australia Telescope
National Facility
Wideband Correlator.
2 Dec 1999
Preliminary.

Contents.

1.0 Description.

1.1 General.

The ATNF Wideband Correlator is a wide bandwidth, 2048 lag auto-correlator, using the NASA SERC correlator IC[1] along with the correlator card designed for the NRAO Greenbank Telescope[2]. The synchronous, static design along with extensive use if field programmable gate arrays allows for lower bandwidth by either simply reducing the system clock rate or by data decimation. By the installation of a second input Data Buffer Card a crosscorrelator can be implemented. At maximum clock rate, the correlator is capable of processing up to 2.048GHz bandwidths[3].
Data flow is from the Samplers, through the Data Buffer card, to the Correlator card, to the Accumulator card, thence to an external the Correlator Control Computer (CCC) for further processing and archiving.
Low level hardware configuration and control is with a small PC based Block Control Computer (BCC) with an onboard ATNF Event Generator. The BCC is in turn command driven by the CCC. An ATNF Distributed Clock is used to tie all timings to the Observatory time base.

Key features:
- Up to 2.048GHz bandwidth[3].
- Clock rate variable bandwidths.
- Precise, flexible control through the use of the ATNF Distributed Clock system.

1. John Canaris/ Mike Davis
2. Ray Escoffier NRAO Central Development Laboratory, Charlottesville West.Virginia USA.
3. Anticpated maximum bandwidth.

1.2 Specifications.

Description	Value	Units
Maximum Correlator Clock Rate	128	MHz.
Maximum number of Lags (auto-correlation - Max BW)	2048	Lags.

Maximum number of Lags (cross-correlation - Max BW)	+/-1024	Lags.
Data Buffer Memory size	4	Mbyte.
Correlator data output rate	20	MHz.
Accumulator Memory size (per bank)	4	Mbytes.
Number of Accumulator Memory banks	2	ea.
Control Timing resolution	1	µS.

1.3 Performance and Operational Constraints.

There are many factors that will limit the performance of the correlator or will require a balance between conflicting options. These include:

i. Correlator Resolution.
ii. Data output rate,
iii. Accumulator Memory size.
iv. Accumulator Width.
v. Sample Count Access.

1.3.1. Correlator Configuration and Resolution - fully populated card.

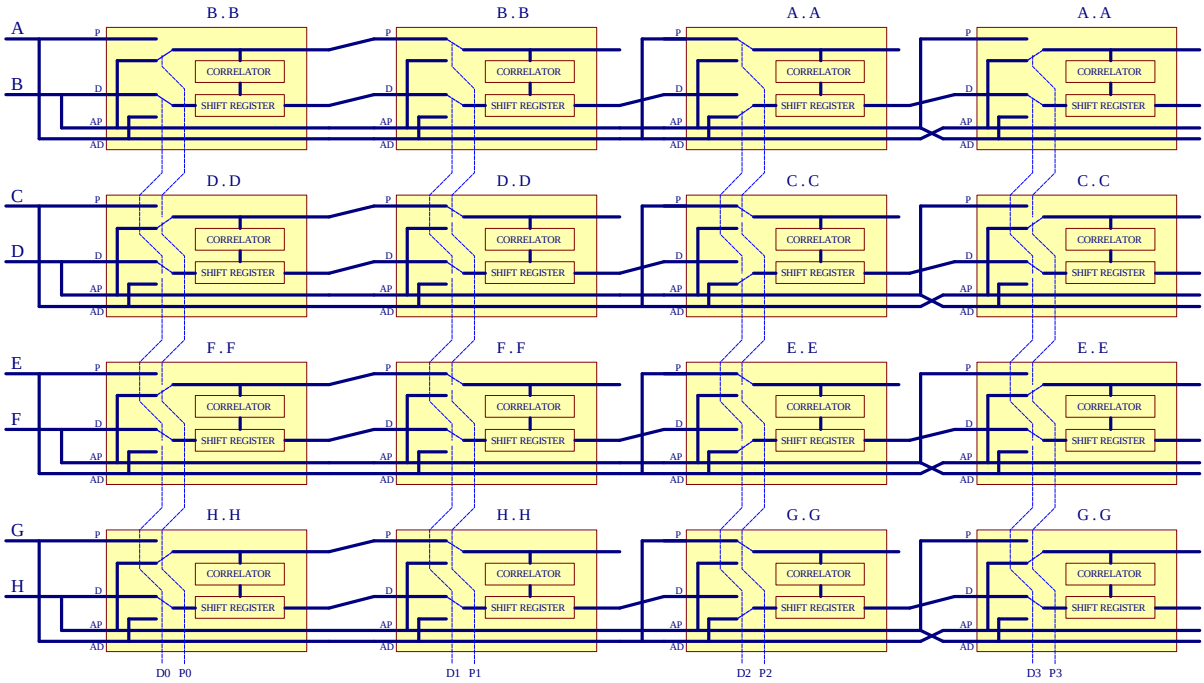
The 16 correlator ICs on each card are interconnected in such a way as to allow the combinations listed below.

	Autocorrelation			Crosscorrelation			Bandwidth	
	N	Lags	Fc	N	Lags	Fc	Contribution.	Products
1	8	2048	2048				512MHz.	A^2 ,B^2 ,C^2 ,D^2 ,E^2 ,F^2 ,G^2 ,H^2.
2	4	4096	4096				256MHz.	B^2 ,D^2 ,F^2 ,H^2.
3	4	4096	4096				256MHz.	A^2 ,C^2 ,E^2 ,G^2.
4	8	1024	1024	4	±1024	1024	256MHz.	A^2 ,B^2 ,C^2 ,D^2 ,E^2 ,F^2 ,G^2 ,H^2. A•B, C•D, E•F, G•H.
5				4	±2048	2048	256MHz.	A•B, C•D, E•F, G•H.

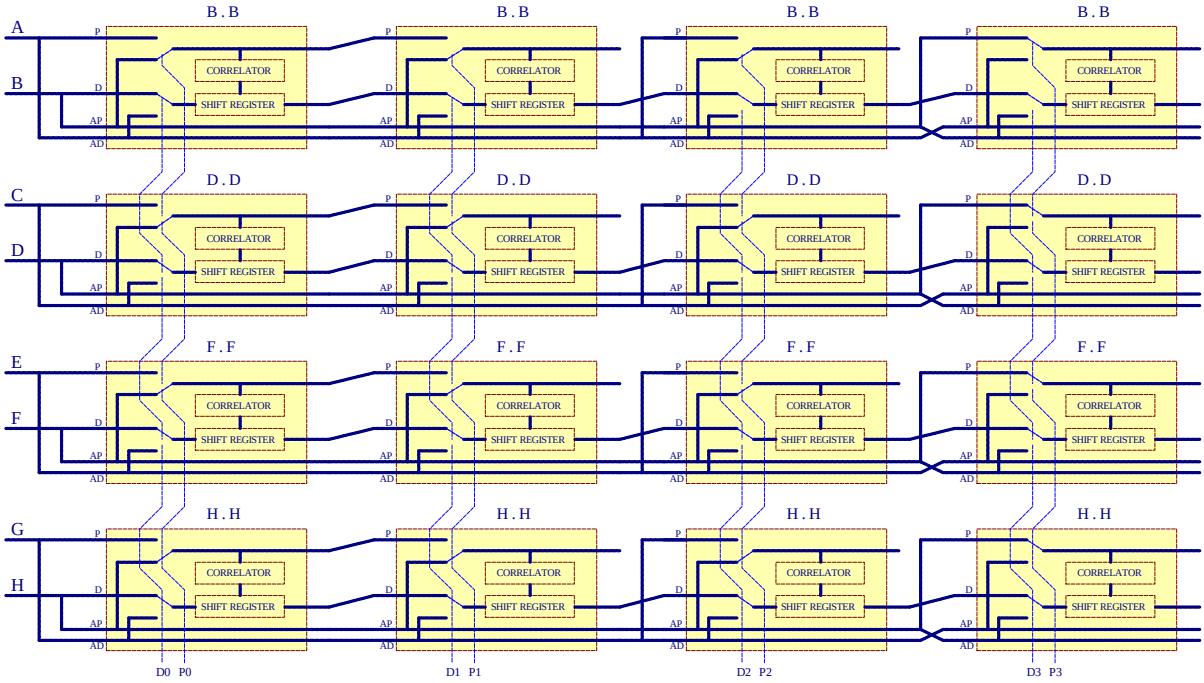
Bandwidth Contribution is the contribution the combination makes to the entire setup. For example, with a card configured for 8 X 2048 Auto, four cards are required to form a 2.048GHz correlator.

The five possible configurations are shown in the following diagrams. In all cases the input signals designated A - H can be selected from any of the 8 signals fed to the accumulator/correlator card.

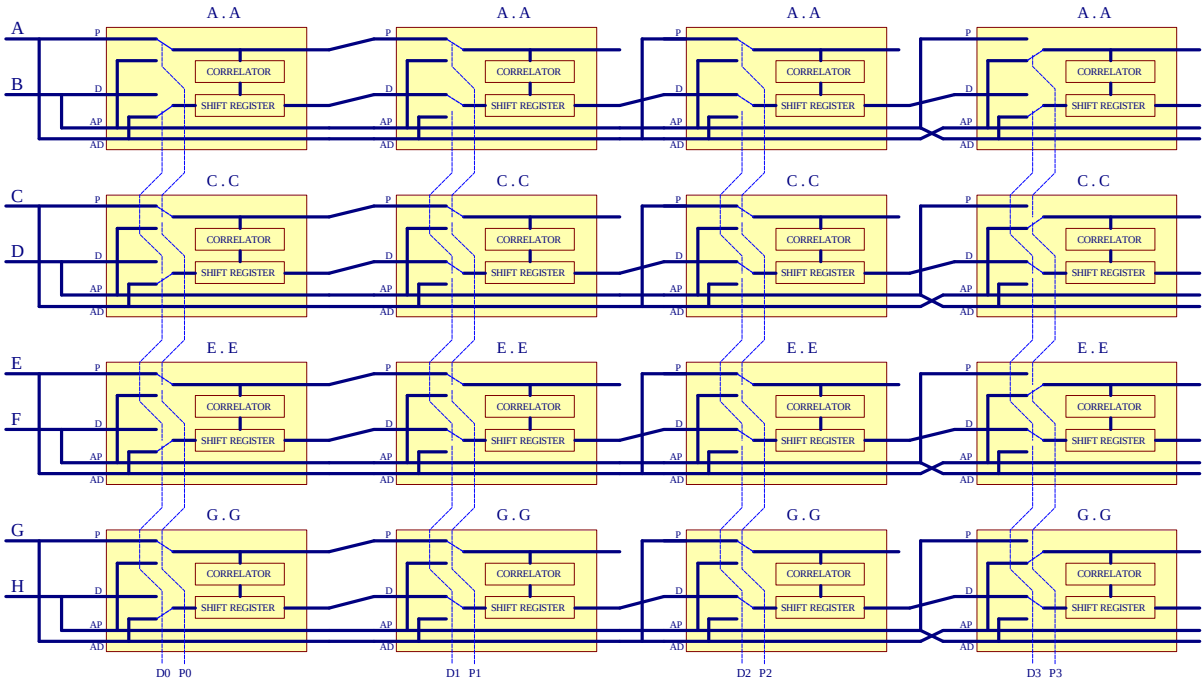
AUTOCORRELATION 8 IFs X 2048 FREQ.CH



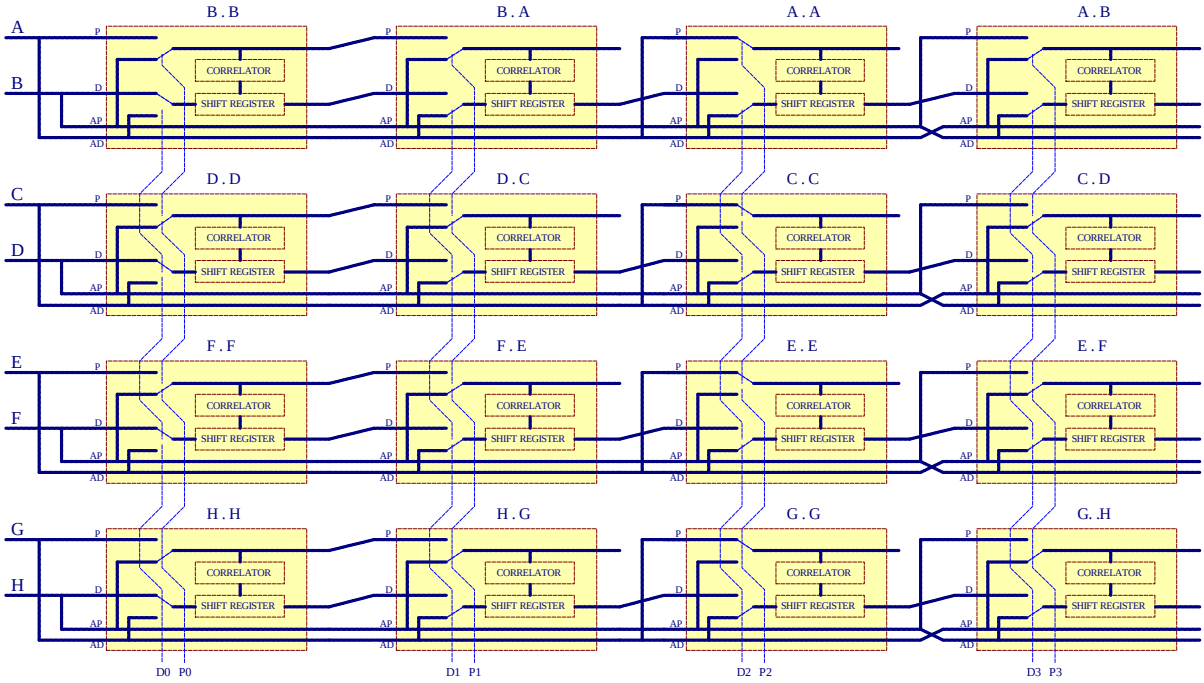
AUTOCORRELATION 4 IFs X 4096 FREQ.CH #1

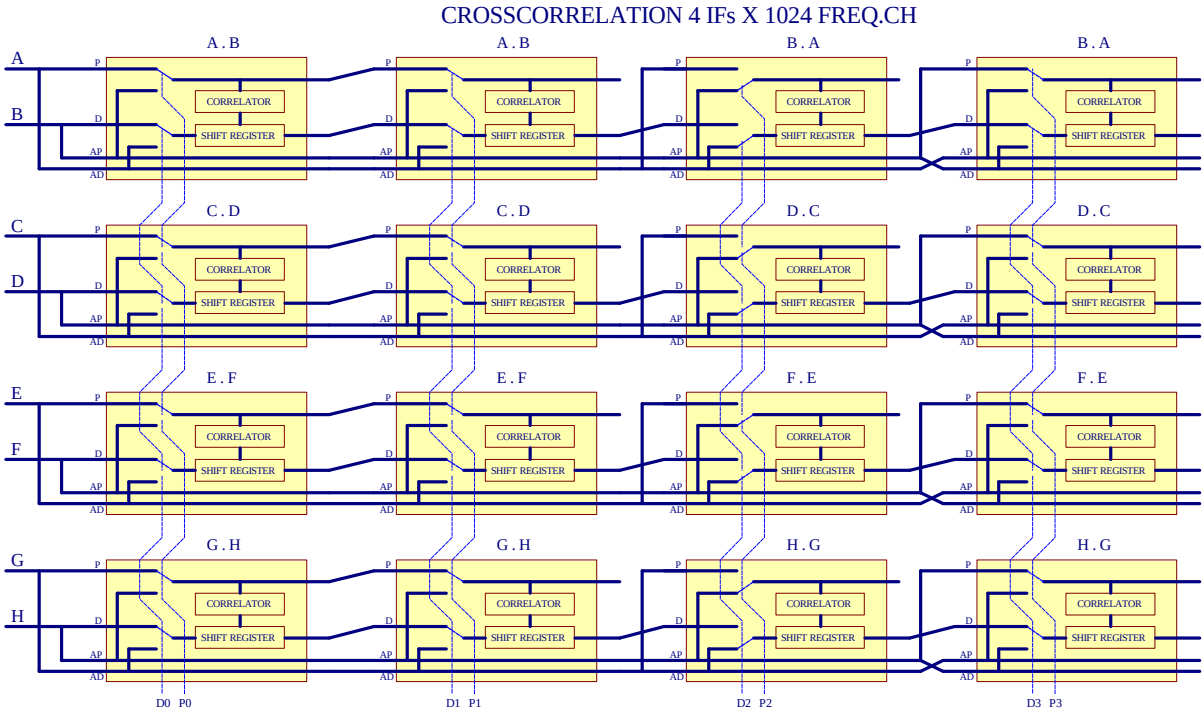


AUTOCORRELATION 4 IFs X 4096 FREQ.CH #2



AUTOCORRELATION 8 IFs X 1024 FREQ.CH & CROSSCORRELATION 4 IFs X 1024 FREQ.CH





1.3.2. Correlator Configuration and Resolution - half populated card.

If each correlator card is only half populated, some performance gains in the data handling area can be made. The disadantages of a half populated card are:

- loss of the higher resolution option of 4096 frequency channels in autocorrelation. All the other configurations should be possible.
- cost and complexity of double the number of correlator cards. This includes additional EURO card bins, power supplies, rack room and cooling.

On the other hand, the advantages are:

- reduced thermal density,
- halves the total dump times of data from correlator IC to the accumulator,
- doubles the accumulator memory available per correlator IC.

There is no change in the performance of the data transfer time from the correlator to the CCC.

1.3.3 Data output rate.

The output data rate of the correlator cards is limited by 3 things. These are: the maximum rate from which data can be shifted from the correlator ICs, the shared or common data path between the correlator ICs and the accumulator, and the shared data path between the Accumulator and the external Correlator Control Computer.

1.3.3.1. The maximum rate that data can be shifted out from the correlator ICs is 20MHz, or one (32 bit) word every 50nS. Thus the Maximum Output Data rate is:

Maximum Output Data rate = Number of Lags X 50nS.

For example, to recover all 1025 (1024 lags + 1 sample counter) would require 50 X 1025 nS, ie 51.25µS, and for say 128 lags it would require 128 X 50 nS, ie 6.4µS. This constraint will limit the minimum continuous integration time.

1.3.3.2. The output data path between the Correlator ICs and the Accumulator, for a given Correlator card, is shared by up to 16 correlator ICs. As data transfers from a single Correlator IC occupies 100% of this bus' bandwidth, the Total Data Transfer Time will be:

Total Data Transfer Time = Correlator ICs in use X No. Lags X Data Rate.

For example, to recover 128 lags from any one correlator IC at 50nS/word will take 6.4μS. If there are 16 correlator ICs in use on a particular Correlator Card, then the Total Transfer Time will be: 16 X 128 X 50nS, ie 102.4μS. This constraint will limit the minimum continuous integration time. For narrower bandwidths, fewer Correlator ICs will need to be used on each card, thus reducing the minimum continuous integration time.

1.3.3.3. The shared data path between the Accumulator and the external Correlator Control Computer (CCC) carries all the data from the correlators into the CCC. It's maximum data rate is around 2 (32 bit) words/μS. Assuming there are no delays in the CCC, then the time to download the data from any accumulator will be:

Download Time = (Number of Lags / 2) μS.

This constraint will limit the minimum continuous integration period.

1.3.4 Accumulator Memory size.

The number of lags and bins that can be processed by the Accumulator is limited by the Accumulator's Memory size. The Memory Size will be:

Lags per Bin X No. of Bins X Correlator ICs in use = Memory Size.

For example, for 128 lags per bin, and 1024 Bins using 16 correlator ICs , would require:

128 X 1024 X 16 = 2MWord = 8MBytes.

As the Accumulator Memory size may vary depending upon the memory device availability, consult the values for the card that will be used.

1.3.5 Accumulator Width.

The largest integer that the Correlator IC will handle is 32 bits. At lag zero, auto-correlation, an overflow will occur after 2**31 correlations. Therefore the maximum time between dumps from the Correlator ICs to the external Accumulator or the CCC will be:

Max Dump Time = 2**31 / Clock Rate.

For example, for a clock rate of 128MHz the Maximum Dump Time will be:

2**31 / 128X10**6 = 16.77 Sec.

If longer integration times are required either scale the data from the Correlator ICs before the Accumulator, or dump the data to the CCC and accumulate the results there.

1.3.6. Sample Count Access.

This value will not be available if more than half the Accumulator memory is allocated or less than 1025 values are transferred from the Correlator ICs.

2.0 Programming.

2.1. Memory model.

2.1.1. CCC Bus.

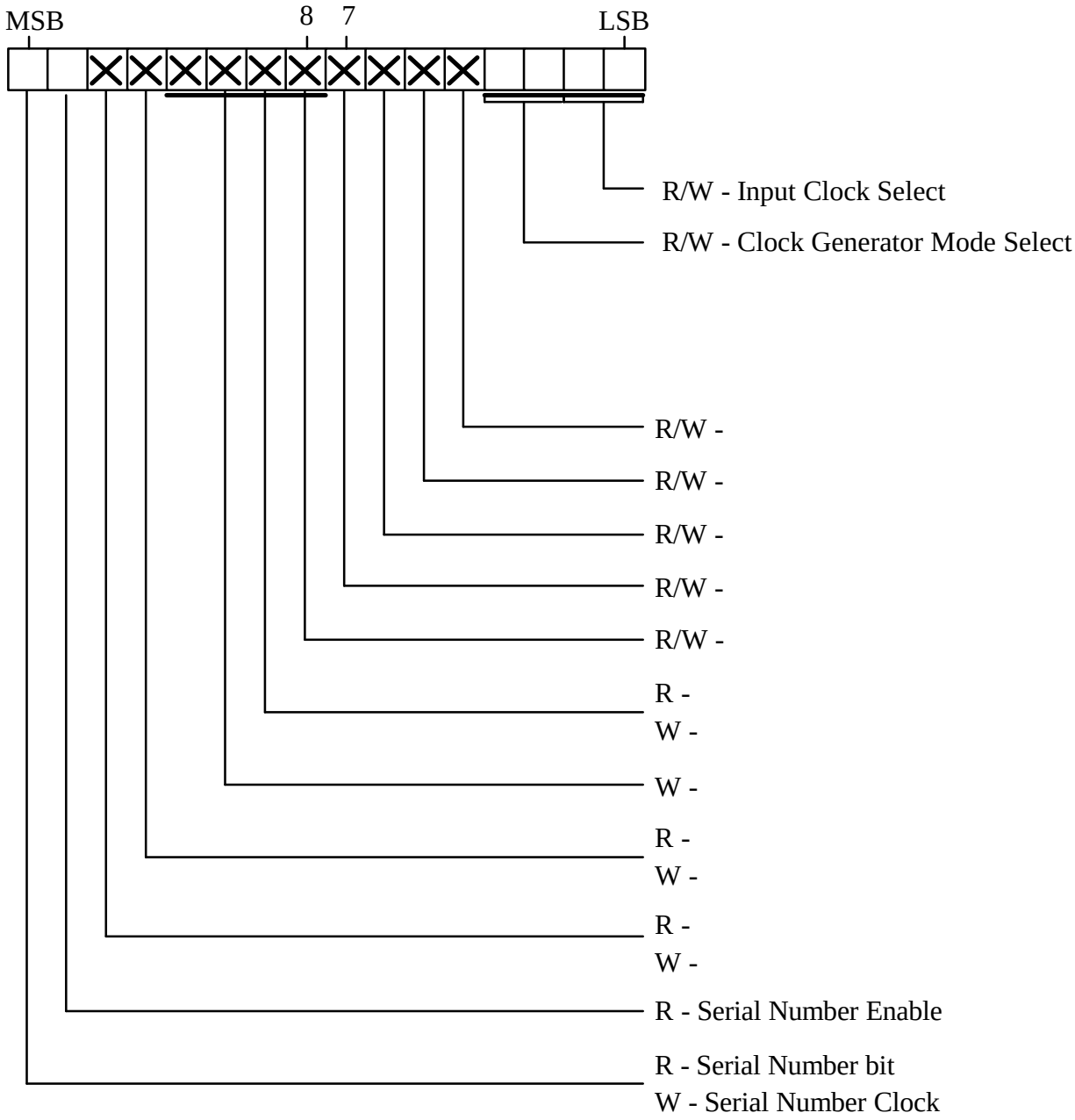
The accumulator is accessable from the CCC on a special purpose bus. This bus is a 32 bits wide combined address and data bus. The interface card residing in the CCC handles the entire transfer with only minimal CCC program intervention. Only word (32 bit) transfers are done.
Each Correlator Block has eight slots, and each slot is designed to accomodate up to 64Mwords of memory and each has a unique identity within the Correlator Block. Thus each card is mapped to a sequential 64M (2^{26}) space within each Correlator Block and each Correlator Block occupies a 512M (2^{29}) space on the special purpose bus. This leaves the top 5 bits of the address space to define the base address of each Correlator Block which is set by DIP switches on the backplane. Thus there can be up to 32 Correlator Blocks!

2.2. Fixed System.
2.3. FPGA firmware.
2.3.1. General.
With the exception of the 2 FGPA devices used to interface to the BCC on both the Data Buffer Card and the Accumulator card, all other FPGA must be programmed by the BCC before either card can be used. In the case of the Data Buffer card there are a total of 9 devices and for the Accumulator there are 2 devices.

2.3.2. Data Buffer Card.
2.3.2.1. General.
There are 9 FPGA devices made up of 4 pairs and one single. Each set of a pair can be programmed identically (the usual case), or if needs be, can be programmed individually. This means that there must be 5 programming operations performed before the Data Buffer card is fully configured.
To speed the programming operation, the interface between the BCC and the FPGA performs the parallel to serial conversion of the configuration data as well as the clocking of the data into the relevant FPGA.
Data is normally stored in the CCC in an Intel® Hex Format file and when required, is downloaded to the BCC for transfer to the appropriate FPGA. The download operation would require the BCC to first reset the target FPGA, transfer the data to it and on completion check that the ‘Done’ bit has gone Hi.
2.3.2.2. Memory Map.

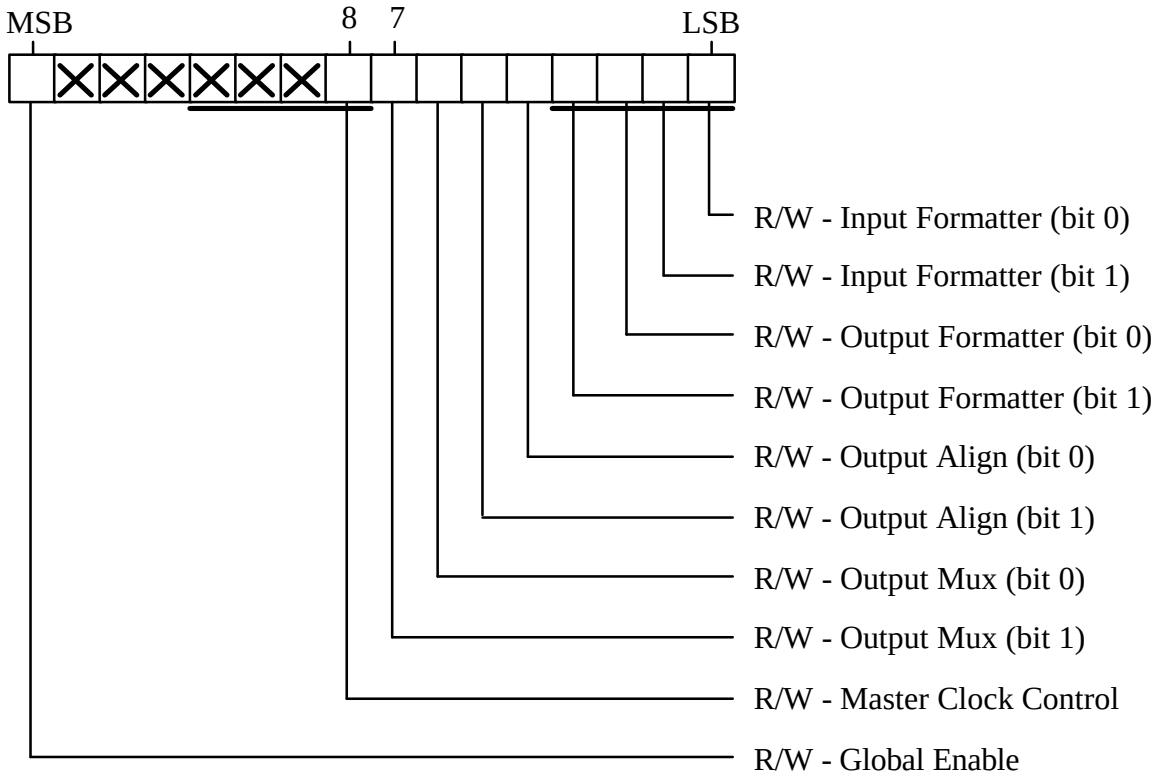
2.3.2.3. Control and Status Register.

CONTROL AND STATUS REGISTER (Offset 0x0)



2.3.2.4. Xilinx Programming Select Register.
This register allows the selection of which Xilinx FPGA to reset and/or program. By setting the appropriate bits, the corresponding Xilinx FPGA will be configured simultaneously. Simultaneous programming is only feasable when the Xilinx FPGA have identical configuration data. To configure a Xilinx FPGA, first set the appropriate bit in this register (as well as the Global Enable bit), then perform a reset by writing to the Xilinx Reset Register, then write the configuration data as 16 bit words into the Xilinx Programming Data Register.

XILINX PROGRAM SELECT REGISTER (Offset 0x1)



Bit	Type	Description
0001	R/W	Input Formatter (bit 0). When set Hi, the control paths to the Xilinx FPGA that handles the input formatting of bit 0 of the data stream from the Samplers into the buffer memory is enabled. This bit must be set Hi to reset and/or program this Xilinx FPGA. The Global Enable bit must also be set Hi.
0002	R/W	Input Formatter (bit 1). When set Hi, the control paths to the Xilinx FPGA that handles the input formatting of bit 1 of the data stream from the Samplers into the buffer memory is enabled. This bit must be set Hi to reset and/or program this Xilinx FPGA. The Global Enable bit must also be set Hi.
0004	R/W	Output Formatter (bit 0). When set Hi, the control paths to the Xilinx FPGA that handles the Output formatting of bit 0 of the data stream from the buffer memory is enabled. This bit must be set Hi to reset and/or program this Xilinx FPGA. The Global Enable bit must also be set Hi.
0008	R/W	Output Formatter (bit 1). When set Hi, the control paths to the Xilinx FPGA that handles the Output formatting of bit 1 of the data stream from the buffer memory is enabled. This bit must be set Hi to reset and/or program this Xilinx FPGA. The Global Enable bit must also be set Hi.
0010	R/W	Output Align (bit 0). When set Hi, the control paths to the Xilinx FPGA that handles the Output aligning of bit 0 of the data stream from the buffer memory is enabled. This bit must be set Hi to reset and/or program this Xilinx FPGA. The Global Enable bit must also be set Hi.
0020	R/W	Output Align (bit 1). When set Hi, the control paths to the Xilinx FPGA that handles the Output aligning of bit 1 of the data stream from the buffer memory is enabled. This bit must be set Hi to reset and/or program this Xilinx FPGA. The Global Enable bit must also be set Hi.
0040	R/W	Output Multiplexer (bit 0). When set Hi, the control paths to the Xilinx FPGA that handles the multiplexing of bit 0 of the data stream from the buffer memory to the

output cables is enabled. This bit must be set Hi to reset and/or program this Xilinx FPGA. The Global Enable bit must also be set Hi.

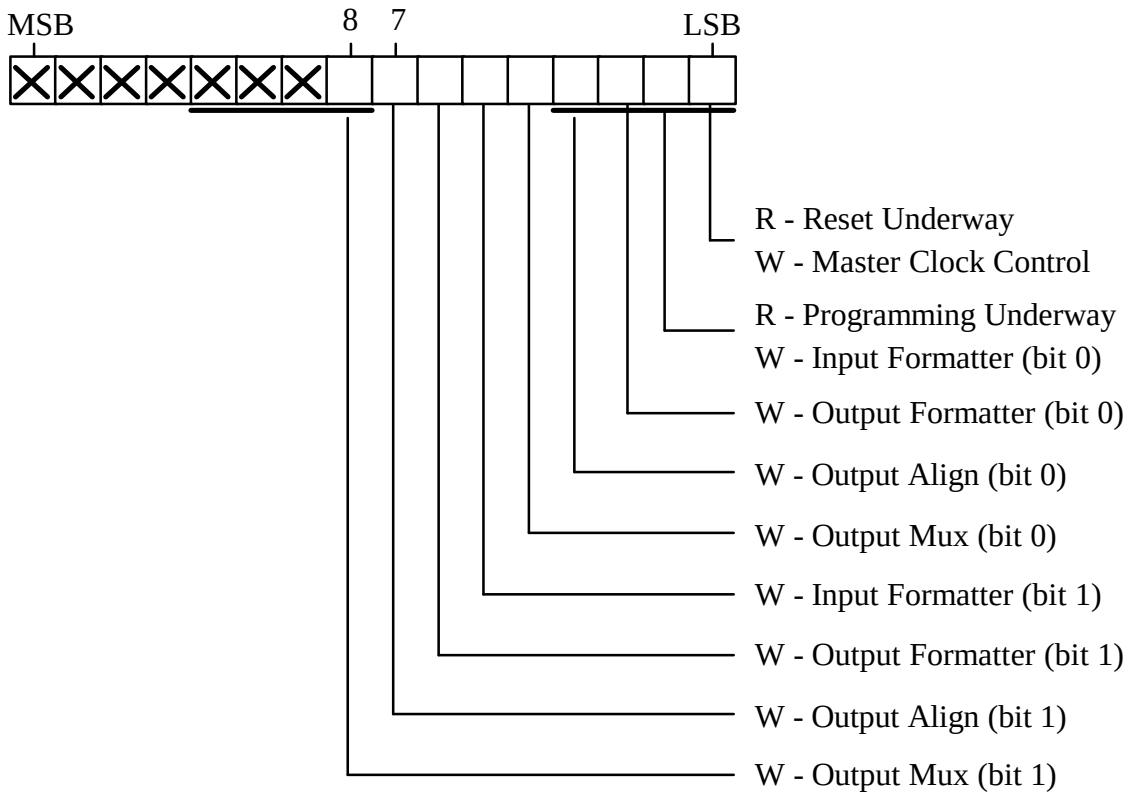
0080 R/W Output Multiplexer (bit 1). When set Hi, the control paths to the Xilinx FPGA that handles the multiplexing of bit 1 of the data stream from the buffer memory to the output cables is enabled. This bit must be set Hi to reset and/or program this Xilinx FPGA. The Global Enable bit must also be set Hi.

0100 R/W Memory Controller. When set Hi, the control paths to the Xilinx FPGA that handles the buffer memory controller is enabled. This bit must be set Hi to reset and/or program this Xilinx FPGA. The Global Enable bit must also be set Hi.

2.3.2.5. Xilinx Reset Register.

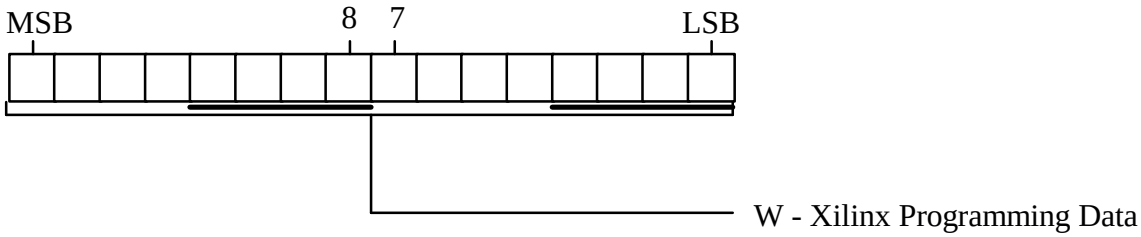
This register allows one or any of the programmable Xilinx FPGAs to be reset. The appropriate bit must also be set in the Xilinx Programming Select Register.

XILINX RESET REGISTER (Offset 0x2)



2.3.2.6. Xilinx Programming Data Register.

XILINX PROGRAMMING DATA REGISTER (Offset 0x3)



2.3.3. Accumulator Card.

2.3.3.1. General.

There are 3 FPGA devices on this board; one for the BCC & Event Generator interface, and the other two form each bank of the accumulator. Both the FPGA that form the accumulator are programmed identically, with individual monitoring of the 'Done' line for diagnostic reasons. This means that there must be a programming operations performed before the Accumulator card is operational.

To speed the programming operation, the interface between the BCC and the FPGA performs the parallel to serial conversion of the configuration data as well as the clocking of the data into the relevant FPGA.

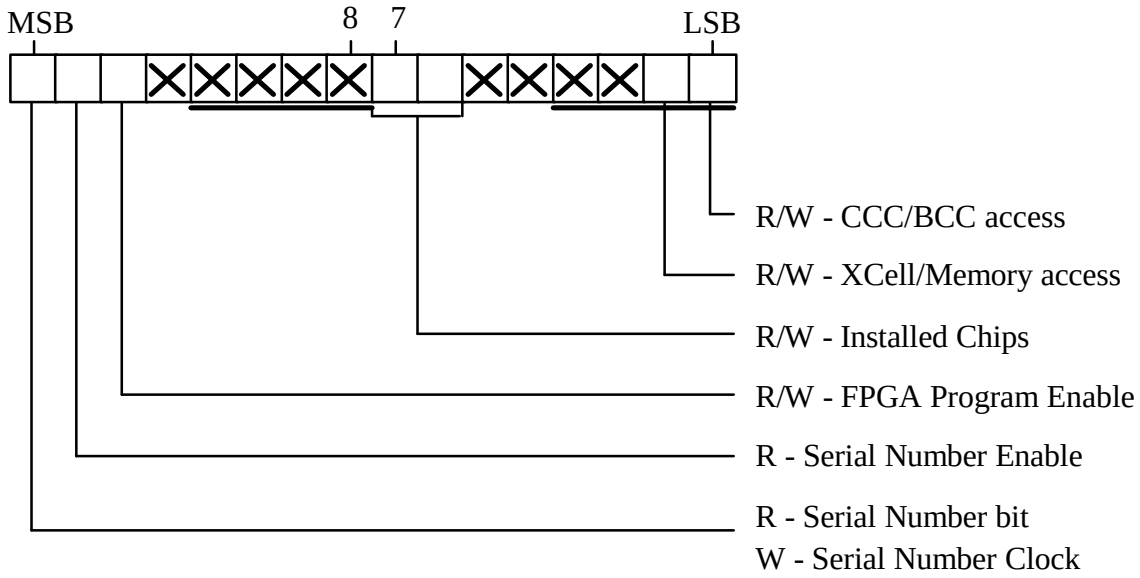
Data is normally stored in the CCC in an Intel® Hex Format file and when required, is downloaded to the BCC for transfer to the appropriate FPGA. The download operation would require the BCC to first reset the target FPGA, transfer the data to it and on completion check that the 'Done' bit has gone Hi.

2.3.3.2. Memory Map

There are 2 sets of registers mapped on the accumulator card; one set is contained in the BCC interface FPGA and the other set contained in the accumulator FPGA. The latter are more nebulus and their access depends upon the mode the accumulators are operating in.

2.3.3.3. Control and Status Register.

CONTROL AND STATUS REGISTER (Offset 0x0)

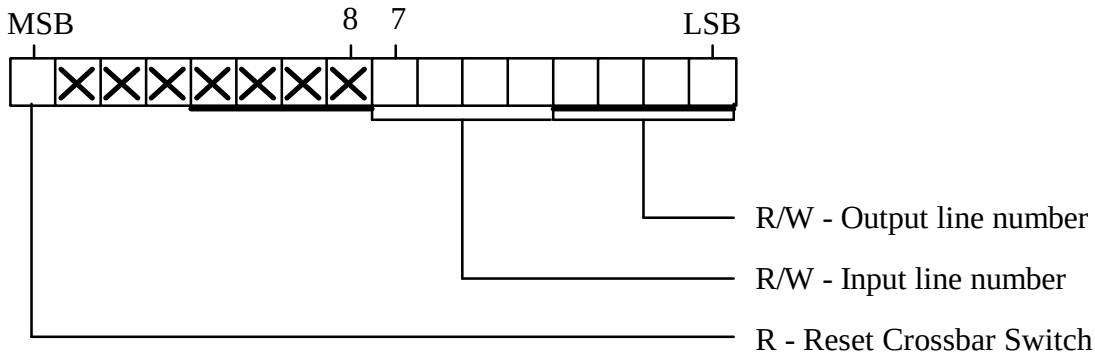


Bit	Type	Description
0001	R/W	CCC/BCC Access. Selects which control computer has access to either the correlator ICs or to the accumulator memory. When set Lo, the Correlator Control Computer (CCC) has access and when set Hi, the Block Control Computer (BCC) has access. Which device is accessed is controlled by the Xcell/Memory Access bit in this register.
0002	R/W	Xcell/Memory Access. This bit selects which device is accessed by the external computers. When set Lo, the XCells are access, and when set Hi, the Accumulator memory is accessed.
00c0	R/W	Installed XCells. These 2 bits define how many correlator ICs are installed on each correlator card. This is: 00 - 2 01 - 4 10 - 8 11 - 16
0c00	R/W	Ext Clock Select. Selects the external clock source for the Correlator from one of the 4 available sources. The Int/Ext Clock Select bit must be set for external Clock.
1000	R/W	Int/Ext Clock Select. Selects the clock source for the Correlator from an external source or from an internal source. The latter choice is principly for testing.
2000	R/W	Xilinx Programme Enable. Enables (or unlocks) access to the control bits that allow configuration of the accumulator Xilinx IC. This bit must be set Hi before any programming operation will work. For safety, set this bit Lo after configuration complete.
4000	R/W	Serial Number Enable. When set Hi the serial number PROM is enabled.
8000	R	Serial Number bit. This is the current bit coming from the Serial Number PROM.
	W	Serial Number Clock. Writing a Hi to this bit advances to the next data bit in the Serial Number PROM. A typical read of the Serial Number PROM would involve first enabling the Serial Number Enable bit (the Serial Number PROM is automatically reset), then repeatedly reading of the Serial Number bit, followed by a single write of a Hi to the Serial Number Clock bit, until the appropriate number of bits has been read.

2.3.3.4. Crossbar Switch Control Register.

The 16 X 16 crossbar switch on the input signals to the correlator card can be set to switch through any input signal to any correlator IC. Bit OR the output line number into the least significant nibble and the desired input line number to the second least significant nubble, and write the result to this register. Note that the Crossbar switch is configured after each write to this register.

CROSSBAR SWITCH CONTROL REGISTER (Offset 0x1)



Bit	Type	Description.
000f	R/W	Output Line Number. Selects which one of 16 output lines of the Crossbar switch to programme.
00f0	R/W	Input Line Select. Switches one of the 16 input lines through to the designated output line.
8000	W	Reset Crossbar Switch. Writing a Hi to this bit will reset the Crossbar switch. This will override any values set in the bottom 8 bits of this register. When reset all the outputs of the crossbar switch are switched to input line 0.

Table of GBT correlator card input signals and corresponding crossbar switch outputs. The GBT signal names are those used on the circuit schematics of that card. It may be also necessary to program the GBT Correlator Card Control Register to select the appropriate GBT Signal.

GBT Signal	CBS output	Comment
+PDATA0	14	⎡ ‘A’ input
-PDATA0	15	⎣
+DDATA0	12	⎡ ‘B’ input
-DDATA0	13	⎣
+PDATA1	10	⎡ ‘C’ input
-PDATA1	11	⎣
+DDATA1	8	⎡ ‘D’ input
-DDATA1	9	⎣
+PDATA2	6	⎡ ‘E’ input
-PDATA2	7	⎣
+DDATA2	4	⎡ ‘F’ input
-DDATA2	5	⎣
+PDATA3	2	⎡ ‘G’ input
-PDATA3	3	⎣
+DDATA3	0	⎡ ‘H’ input
-DDATA3	1	⎣

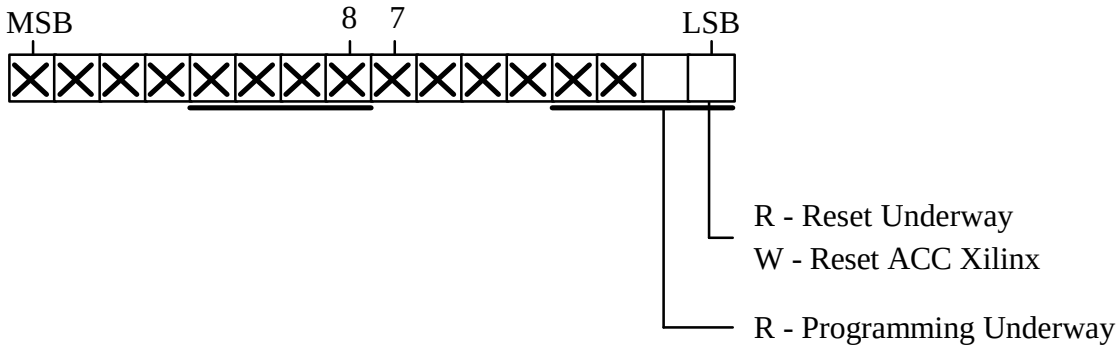
Table of crossbar switch inputs and corresponding signal sources. The source signal numbering starts with 0 from the top most row of pins on the lower EURO connector. In some documentation ‘+’ may be referred to as bit 0, and ‘-‘ as bit 1.

Source signal	CBS input	Comment
+0	15	
-0	10	
+1	14	
-1	9	
+2	13	
-2	8	
+3	12	
-3	7	
+4	11	
-4	6	
+5	5	
-5	2	
+6	4	
-6	1	
+7	3	
-7	0	

As an example, if input signal ‘0’ (both bits) was required to be fed to PDATA0 (both bits), then the values 0x00fd and 0x00af should be written into the Crossbar Switch Control Register.

2.3.3.5. FPGA Programming Control and Status Register.

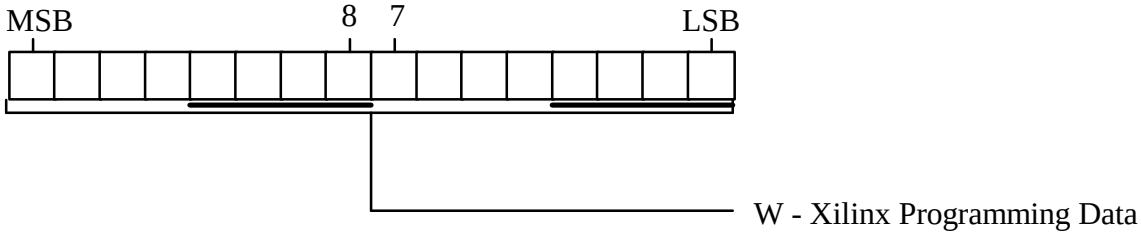
XILINX RESET REGISTER (Offset 0x2)



Bit	Type	Description
0001	R	Reset Underway. When Hi the reset operation is currently underway. Performing any other programming operation on the Xilinx IC during this time may not work.
	W	Reset ACC Xilinx. Writing a Hi to this bit pulses the reset line in both of the Accumulator Xilinx ICs, thus forcing a reset.
0002	R	Programming Underway. When Hi, programming data is being written out the the Accumulator Xilinx ICs. Writing any more data during this time may cause the current data to be corrupted, thus causing the Xilinx configuration process to fail. When configuring a Xilinx IC, do a check on this bit before writing data to the Xilinx programming Data Register.

2.3.3.6. FPGA Programming Data Register.

XILINX PROGRAMMING DATA REGISTER (Offset 0x3)

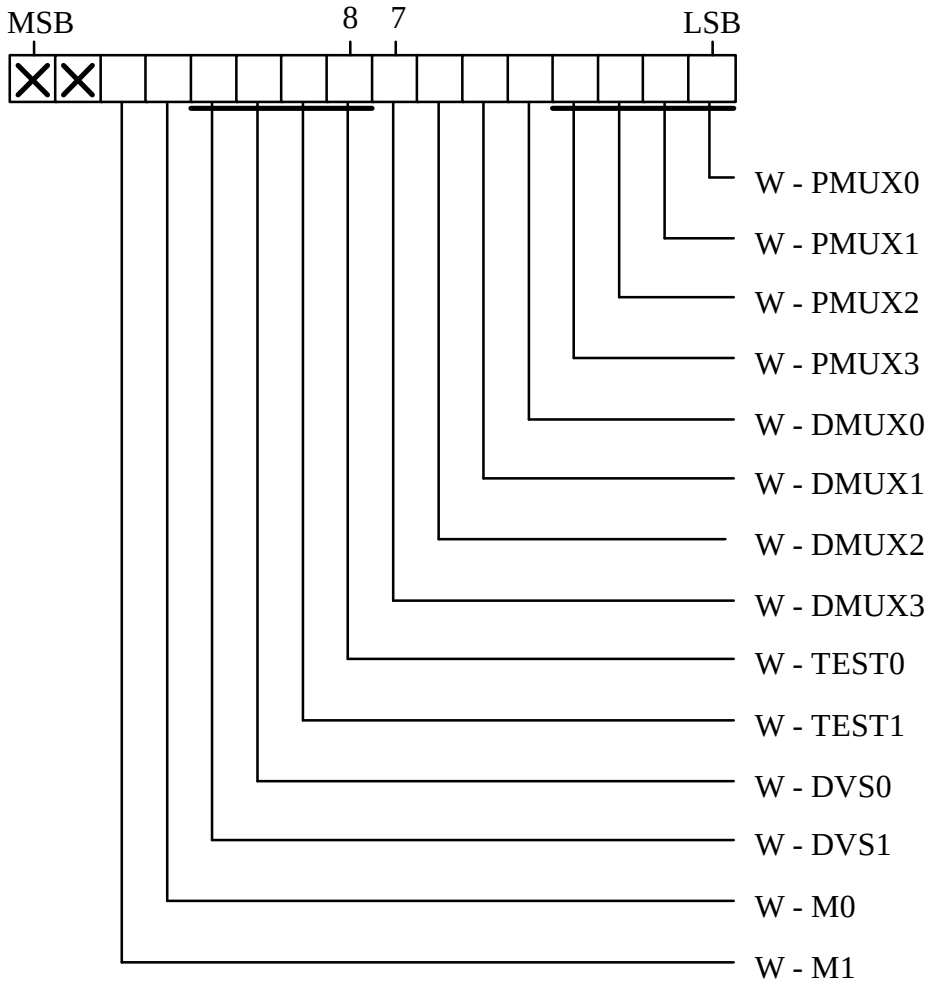


Bit	Type	Description
0001	R	ACC Xilinx #0 Done.When Hi Accumulator Xilinx IC #0 has successfully been configured.
0002	R	ACC Xilinx #1 Done.When Hi Accumulator Xilinx IC #1 has successfully been configured.
ffff	W	Xilinx Programming Data. Each 16 bits of the Xilinx configuration data is loaded into this register. Data is loaded directly as read form an Intel hex format file as a 16 bit integer, for example the first 4 bytes of ASCII data from such a file may be: FF 04 06 98 F9 DA FF FB thus the 16 bit word 0xFF04 will be written on the first pass, 0x0698 will be written on the second pass, etc.

2.3.3.7. GBT Correlator Card Control Register.

The Control register on the NRAO GBT can be programmed by writing to this register. As the register is serially loaded, there may be several microseconds between when data is written and when the bits actually take effect.

GBT CORRELATOR CARD CONTROL REGISTER (Offset 0x4)

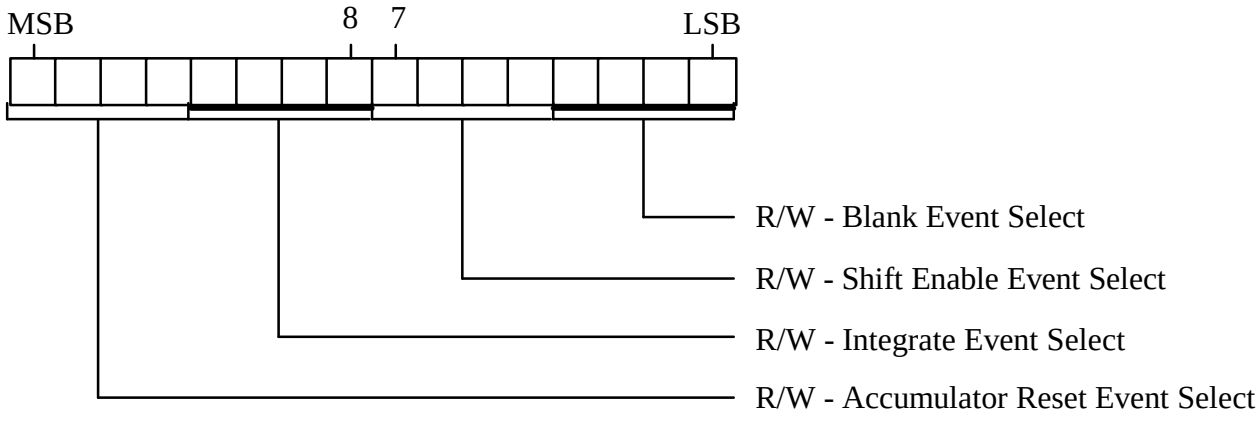


Bit	Type	Description
0001	W	PMUX0. Prompt Input Multiplexer Control for Correlator ICs 2C, 4C, 6C and 8C. When clear the input data that feeds the ‘prompt’ side of the correlator chain enters the correlator IC via the primary inputs, and when set this input data enters the correlator IC via the auxillary inputs.
0002	W	PMUX1. Prompt Input Multiplexer Control for Correlator ICs 2D, 4D, 6D and 8D. When clear the input data that feeds the ‘prompt’ side of the correlator chain enters the correlator IC via the primary inputs, and when set this input data enters the correlator IC via the auxillary inputs.
0004	W	PMUX2. Prompt Input Multiplexer Control for Correlator ICs 2E, 4E, 6E and 8E. When clear the input data that feeds the ‘prompt’ side of the correlator chain enters the correlator IC via the primary inputs, and when set this input data enters the correlator IC via the auxillary inputs.
0008	W	PMUX3. Prompt Input Multiplexer Control for Correlator ICs 2F, 4F, 6F and 8F. When clear the input data that feeds the ‘prompt’ side of the correlator chain enters the correlator IC via the primary inputs, and when set this input data enters the correlator IC via the auxillary inputs.

0010	W	DMUX0. Delayed Input Multiplexer Control for Correlator ICs 2C, 4C, 6C and 8C. When clear the input data that feeds the ‘delayed’ side of the correlator chain enters the correlator IC via the primary inputs, and when set this input data enters the correlator IC via the auxillary inputs.
0020	W	DMUX1. Delayed Input Multiplexer Control for Correlator ICs 2D, 4D, 6D and 8D. When clear the input data that feeds the ‘delayed’ side of the correlator chain enters the correlator IC via the primary inputs, and when set this input data enters the correlator IC via the auxillary inputs.
0040	W	DMUX2. Delayed Input Multiplexer Control for Correlator ICs 2E, 4E, 6E and 8E. When clear the input data that feeds the ‘delayed’ side of the correlator chain enters the correlator IC via the primary inputs, and when set this input data enters the correlator IC via the auxillary inputs.
0080	W	DMUX3. Delayed Input Multiplexer Control for Correlator ICs 2F, 4F, 6F and 8F. When clear the input data that feeds the ‘delayed’ side of the correlator chain enters the correlator IC via the primary inputs, and when set this input data enters the correlator IC via the auxillary inputs.
0100	W	TEST0. Test Control bit for Correlator ICs 2C, 4C, 6C, 8D, 2D, 4D, 6D and 8D. When clear the correlator ICs operate normally, and when set these chips are put into test mode.
0200	W	TEST1. Test Control bit for Correlator ICs 2E, 4E, 6E, 8F, 2F, 4F, 6F and 8F. When clear the correlator ICs operate normally, and when set these chips are put into test mode.
0400	W	DVS0. Double Mode Control bit for Correlator ICs 2C, 4C, 6C, 8D, 2D, 4D, 6D and 8D. When clear the correlator ICs operate at 1:1 speed, and when set these chips are put into double mode where the clock speed is twice the data rate.
0800	W	DVS1. Double Mode Control bit for Correlator ICs 2E, 4E, 6E, 8F, 2F, 4F, 6F and 8F. When clear the correlator ICs operate at 1:1 speed, and when set these chips are put into double mode where the data rate is half the clock speed.
1000	W	M0. When cleared the output buffers on the correlated data bus can be enabled when the card is accessed, and when set the correlated data bus cannot be enabled.
2000	W	M1. This bit goes to the Correlator IC select decode PALs, and currently is not used.

2.3.3.8. Correlator Event Select Register.
This register allows the selection of which event line will be used to drive each of the 4 control lines that drive the Correlator ICs.

CORRELATOR EVENT SELECT REGISTER (Offset 0x5)



Bit	Type	Description
000f	R/W	The binary value of the event line to use to drive the BLANK signal of the Correlator IC array. **Note, this signal is OR'd with the auto blank signal from the Data Buffer Card.**
000f	R/W	The binary value of the event line to use to drive the SHIFT ENABLE signal of the Correlator IC array.
000f	R/W	The binary value of the event line to use to drive the INTEGRATE signal of the Correlator IC array.
000f	R/W	The binary value of the event line to use to drive the ACCUMULATOR RESET signal of the Correlator IC array.

2.3.3.9. Accumulator BCC Read Address Register (LS Word).

Bit	Type	Description
ffff	R/W	If reading from the accumulator memory, this is the LS 16 bit word of the memory to access. If reading directly from the Correlator ICs, the bottom 4 bits are used to select which Correlator IC to access; all the remaining bits in this register and in the Accumulator BCC Read Address Register (MS Word) have no meaning. When reading from the accumulator memory, this register in conjunction with the Accumulator BCC Read Address Register (MS Word), autoincrements with each reading of the MS Accumulator BCC Read Data Register. Thus to transfer a block of data from memory to the BCC, write the 32 bit start address into this and the Accumulator BCC Read Address Register (MS Word), then repeatedly read the Accumulator BCC Read Data Register (LS Word) and the Accumulator BCC Read Data Register (MS Word) **in that order** as many times as necessary.

2.3.3.9. Accumulator BCC Read Address Register (MS Word).

Bit	Type	Description
ffff	R/W	If reading from or writing to the accumulator memory, this is the MS 16 bit word of the memory to access. If reading directly from the Correlator ICs, the contents of this register have no meaning. When reading from the accumulator memory, this register in conjunction with the Accumulator BCC Read Address Register (LS Word), autoincrements with each reading of the MS Accumulator BCC Read Data Register. Thus to transfer a block of data from memory to the BCC, write the 32 bit start address into the Accumulator BCC Read Address Register (LS Word) and this register, then repeatedly read the Accumulator BCC Read Data Register (LS Word) and the Accumulator BCC Read Data Register (MS Word) **in that order** as many times as necessary.

2.3.3.10. Accumulator BCC Read Data Register (LS Word).

Bit	Type	Description
ffff	R/W	This is the LS 16 bit word of the data being read from or written to memory or read directly from the Correlator ICs, depending upon the access mode set**. With both types of access this register must be read or written (if applicable) first**.

2.3.3.10. Accumulator BCC Read Data Register (MS Word).

ffff R/W This is the MS 16 bit word of the data being read from or written to memory or read directly from the Correlator ICs, depending upon the access mode set**. With both types of access this register must be read or written (if applicable) last**.

2.3.3.11. Accumulator BCC StatusRegister.

3.0 Hardware Systems.

3.1.0 Data Buffer Card.

This card buffers the high data rate of the samplers into a form suitable for the much slower speed correlator ICs. This is done by storing the incoming data sequentially into memory, then dividing that data into segments and reading it out to the correlators. Data enters this card on a time contiguous 16 sample wide bus (32 bits in all) at 256 MHz and leaves as 32 separate, time sliced 1 sample wide bus (2 bits) at 128MHz.

The memory block consists of 2 halves. While one half is being written to, the other half can be read from. This form allows much slower memory elements to be used, but requires more memory.

3.1.1. Data input.

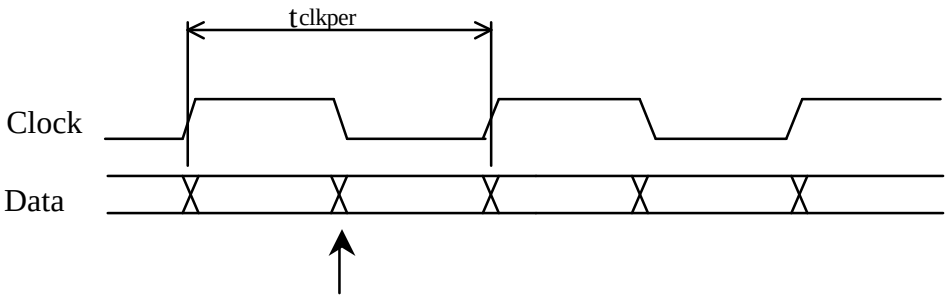
Data is received from the samplers on a 16 sample wide, 32 pair balanced ECL. Data format is shown below. A clock signal, running at half the data rate is also included on an additional pair on each cable. Both the data and the clock should change state at the same instant. (The clock signal should be treated as an ordinary data line by the driving end). Transmission of the correlator clock with the data will always guarantee correct phase relationship between it and the data regardless of frequency and cable length.

The physical cable consists of two halves, each made up of 34 way (17 pair) twisted pair ribbon cable (such as Spectra Twist'N'Flat cable) with a characteristic impedance of around 100Ω. Cable #1, carries samples 0 through to 7 on pairs 1 through to 16 respectively, and on cable #2 samples 8 through to 15 on pairs 1 through to 16 respectively. On both cables, pair 17 carries the clock. Sample 0 is deemed to have occurred at t = 0, sample 1 at t = 1, etc. Each set of cables should be within several centimetres of the same length.

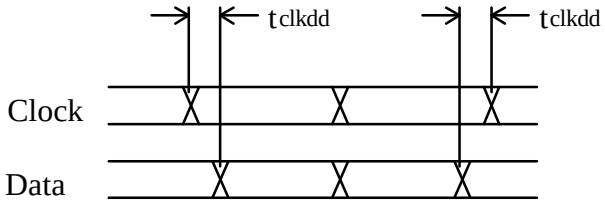
Transfer of the signals from the cable to the buffer card is by direct connection to DIN 41612 connector pressed into the motherboard. This connector is of the loadable pin crimp type.

Table 1. Sampler-Correlator Cable Pin assignment.

Wire	Cable #1 Signal	Cable#2 Signal	Comment
1	S0-D0	S8-D0	
2	~S0-D0	~S8-D0	
3	S0-D1	S8-D1	
4	~S0-D1	~S8-D1	
5	S1-D0	S9-D0	
6	~S1-D0	~S9-D0	
7	S1-D1	S9-D1	
8	~S1-D1	~S9-D1	
9	S2-D0	S10-D0	
10	~S2-D0	~S10-D0	
11	S2-D1	S10-D1	
12	~S2-D1	~S10-D1	
13	S3-D0	S11-D0	
14	~S3-D0	~S11-D0	
15	S3-D1	S11-D1	
16	~S3-D1	~S11-D1	
17	S4-D0	S12-D0	
18	~S4-D0	~S12-D0	
19	S4-D1	S12-D1	
20	~S4-D1	~S12-D1	
21	S5-D0	S13-D0	
22	~S5-D0	~S13-D0	
23	S5-D1	S13-D1	
24	~S5-D1	~S13-D1	
25	S6-D0	S14-D0	
26	~S6-D0	~S14-D0	
27	S6-D1	S14-D1	
28	~S6-D1	~S14-D1	
29	S7-D0	S15-D0	
30	~S7-D0	~S15-D0	
31	S7-D1	S15-D1	
32	~S7-D1	~S15-D1	
33	Clock	Clock	
34	~Clock	~Clock	
35	GND	GND	(optional for 40 way cable)
36	GND	GND	(optional for 40 way cable)
37	GND	GND	(optional for 40 way cable)
38	GND	GND	(optional for 40 way cable)
39	GND	GND	(optional for 40 way cable)
40	GND	GND	(optional for 40 way cable)



SAMPLER-CORRELATOR DATA FORMAT

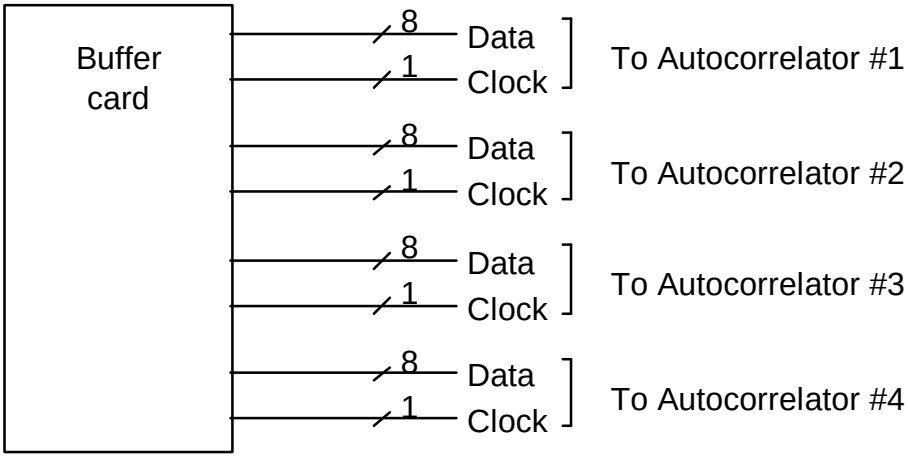


SAMPLER-CORRELATOR DATA-CLOCK TIMING

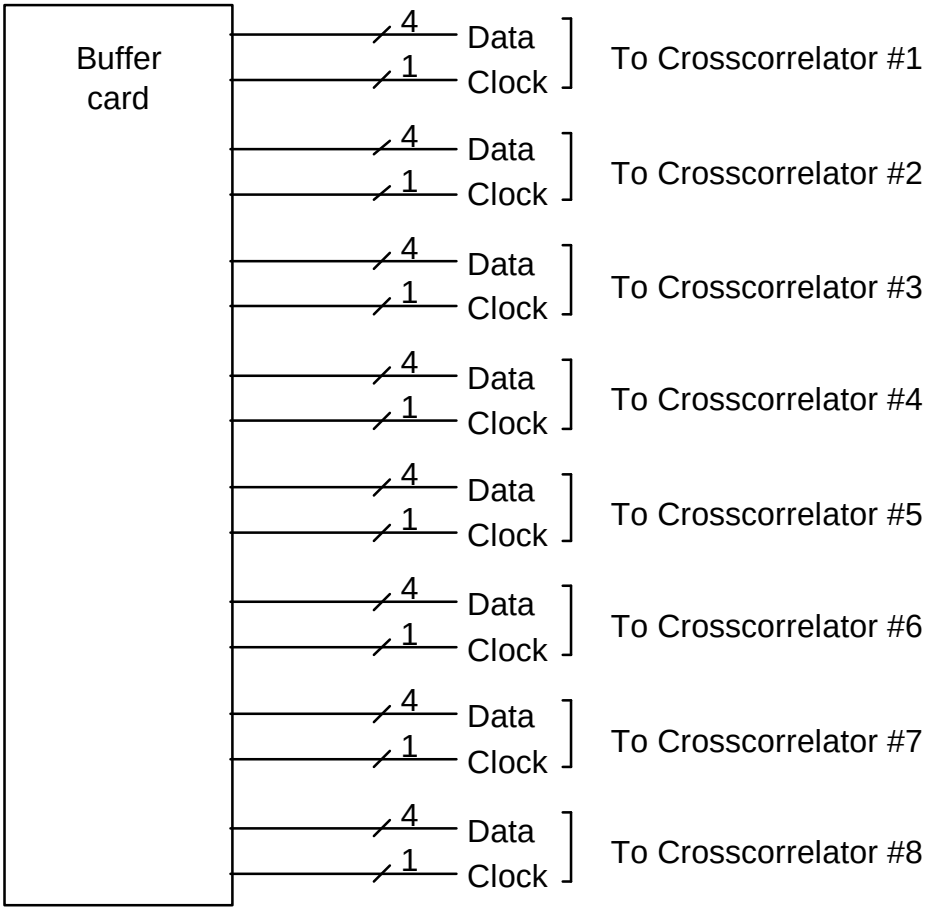
Name	Symbol	Min	Typ	Max	Units
Clock Period	t_{clkper}	7.8	-	-	nS
Clock-Data delay	t_{clkdd}	-0.25	0	0.25	nS

3.1.2. Data Output.

Data leaves the Buffer card on 32 separate data buses, each made up of 2 bits in balanced ECL. Appropriate cabling is required to take the data from the Buffer card to the correlator card. There is also 8 clock outputs available at the output connector. Depending upon the correlator system required, different cable arrangements can be easily assembled. Transfer of the signals to the cable from the buffer card is by direct connection to the DIN 41612 connector pressed into the motherboard. This connector is of the loadable pin crimp type. The availability of the 8 clock outputs, allows for a simple maximum bandwidth correlator autocorrelator which would require 4 correlator cards (4 clocks) or a maximum bandwidth crosscorrelator which would require 8 correlator cards (8 clocks).



BUFFER CARD CABLING OUTPUT FOR 4 AUTOCORRELATORS



BUFFER CARD CABLING OUTPUT FOR 8 CROSSCORRELATORS

All 32 X 2 bit data buses are aligned, so that at the data on them changes to the new data at the same instant after a change from one memory bank to another. A balanced TTL “Blank” signal, lasting 16?

clock periods, is issued at the changeover point to inform all boards receiving this data that a discontinuity in the data has occurred. The boards receiving the data should use this signal to blank their correlators for the appropriate period.

3.1.3. Runtime Control.
Runtime Control is done by one signal. This signal resets the memory control sequencer which in turn restarts the loading process. Once reset the memory control sequencer runs continuously accepting data from the samplers and sending data to the correlators. The Buffers must run at least one load cycle before the data to the correlators is valid.

3.1.4. Configuration.
The Buffer card can be configured for many different forms of operation. FPGAs are used extensively in the data path and sequence controller. These can be programmed from an external computer (BCC) during system configuration. A "master" FPGA is used as the interface between the external control computer and the other FPGAs.

3.2.0 Correlator Accumulator Card.
3.2.1 General.
The Correlator Accumulator card physically sits between the Correlator Card and the system backplane. It performs the following functions:
1. An interface between the Buffer card's output cabling and the Correlator card.
2. Clock generator for the Correlator card.
3. An interface between the ATNF control system and the Correlator Card,
4. A temporary accumulator for the Correlator data output.

3.2.2. Interface between the Buffer card's output cabling and the Correlator card.
Signals enter this card from the one or two Buffer cards as balanced ECL. The signals are then passed through a crosspoint switch which allows any data stream into the correlator to be selected from any of the data lines coming from the buffer card. This will allow a variety of configurations to be enabled quite easily. After the data has emerged from the crosspoint switch, it is re-synchronised then converted to single ended ECL and then passed to the Correlator card.

3.2.3. Clock generator for the Correlator card.
The correlator clock is sent with the data from the Buffer card. The timing of the clock is similar to that between the Samplers and the Buffer card; the edge of the clock signal is aligned with the change in the data. See the timing diagram for timing constraints. There is very little processing of the clock signal, other than inserting a delay, and appropriate buffering. All re-synchronising is then done with this delayed and buffered clock signal. The clock signal is also divided down by either 2X or 4X converted to TTL and fed to the master FPGA. This allows the existence of the clock signal to be monitored as well as phase locking an on board VCO for complete system synchronisation.

3.2.4. Interface between the ATNF control system and the Correlator Card,
There are 2 parts to this section; the general configuration function, and the runtime control function. The general configuration function, allows the BCC to configure the hardware, both on this card and the attached NRAO Correlator Card. This includes signal data path selection, input clock selection, Event Generator signal selection, configuration of the Accumulator FPGAs as well as Accumulator functional setup, and the configuration of the registers on the NRAO Correlator card. As the FPGAs that make up the Accumulator are interconnected to the internal PCC bus, correlated data may be read directly from the Correlator ICs or from the accumulator by the BCC.
The run-time control toggles the various Event Generator signals and other signals including the Blank signal from the Buffer card. Some run-time control will come from the Event Generator, and

some will be automatically generated on the card. For any rapid switching, such as with short Pulsar periods or the like, the control signals will need to be generated by some automatic means such as internal counters or a digital signal synthesiser, as the current ISA ATNF Event Generator can only generate events at a sustain rate of one every 100-200nS. The final configuration may be determined by the functionality designed into the various FPGA's firmware.

3.2.5 Temporary Accumulator.

The temporary accumulator accumulates correlated data in a separate buffer to that built into the Correlator ICs. While not necessary for simple correlation strategies, the Accumulator is necessary whenever very long integrations are required, or whenever the data must be time sliced, such as with Pulsar binning, noise calibration signal use etc.

For simple correlation, the accumulator may be completely by-passed, so that the CCC directly reads the buffers built into the Correlator ICs.

The Accumulator is made up of 2 (near) identical banks. There status is defined by a common signal such that when in one state, Bank "A", is accumulating, while Bank "B" can be accessed by the CCC, and when in the other state, Bank "A" can be accessed by the CCC, while Bank "B" is accumulating.

Each bank of the Accumulator memory is made up of 4 X 72 pin SIMMs. Into each of these SIMMs high speed static memory modules can be installed. The current design calls up modules of 32 X 256K each, giving each bank a total capacity of 4MB, or 1Mword. The speed of the memory is dependent on the data transfer/accumulator rate from the correlator ICs and the speed of the Accumulator FPGA ICs. For maximum data transfer/accumulator rate from the correlator ICs, and medium speed FPGAs a read or a write cycle must take less than ~20nS. Thus a memory speed of faster than this would be required. With the medium speed FPGAs pipelining of the addition operation is required. This means that reads from a series of correlator ICs, will need to have a short delay between them. See the section titled "Performance and Operational Constraints" for understanding limitations on functionality for a given amount of accumulator memory.

3.3. Power Consumption.

The Power consumption of the correlator system is frequency dependant.

3.3.1. Data Buffer card.

Nominal power requirements (amps):

	+5V	-2V	-5.2V	Power(W)	Comment
Standby	2.1	1.7	3.1		All logic configured, no clock.
1GHz B/W	6.0	1.8	3.2		
2GHz B/W	9.9	1.9	3.3	70.5	Estimated

3.3.2 Accumulator/Correlator card combination.

The following is the power requirements for an Accumulator/Correlator card combination with 8 correlator ICs and one SIMM in the accumulator running in a basic mode. A typical basic mode would include 12Hz dump rate to the accumulator, and an integration time of 5 seconds. Increasing the dump rate will cause an increase in current demand.

Nominal power requirements (amps):

	+5V	-5.2V	Power(W)	Comment
Standby	4.6	4.2		All logic configured, no clock.
1GHz B/W	6.5	4.1		
2GHz B/W	8.4	4.2	63.8	Estimated

Appendix A.

Buffer Card Clock Generation Timing Analysis.

Synchronous design techniques has been implemented in the design of the buffer card as much as possible. This method removes many (but not all) of the subtle delays required in the various clocks around the board. This appendix is an analysis of the timings of the various clocks and data streams on the board.

1.0 Input Section.

This stage takes the 256MHz ECL data from the cable, broadens it out and slows it down to 128MHz TTL. The master clock signal is supplied with the data. It has a frequency of half the data rate. The maximum data rate is 256M bits per second. Thus the maximum incoming clock rate is 128MHz.

To de-multiplex the data both the rising edge and the falling edge are use to clock the data into holding registers. The master clock signal's edges are co-incident with the data edges. Figure A1 shows the input stage.

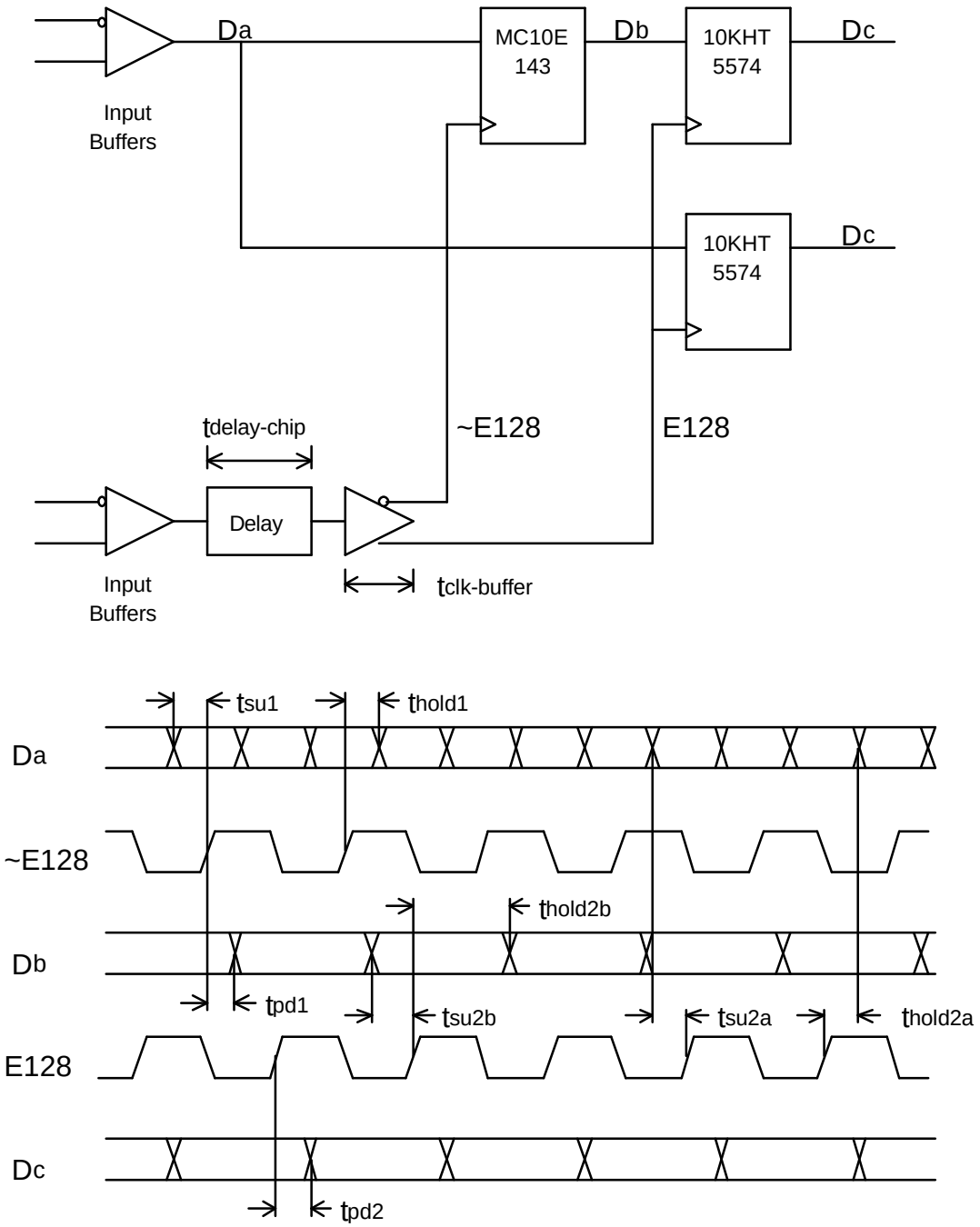


FIGURE A1
INPUT STAGE TIMING (ECL Clocks)

Name	Symbol	Min	Typ	Max	Units
Raw Data Setup[1]	t_{su1}	50	-100		pS
Raw Data Hold[1]	t_{hold1}	300	100		pS
Propagation delay[1]	t_{pd1}	600		1000	pS
Raw Data Setup[2]	t_{su2a}	1000			pS
Raw Data Setup[2]	t_{su2b}	1000			pS
Raw Data Hold[2]	t_{hold2a}	1000			pS
Raw Data Hold[2]	t_{hold2b}	1000			pS
Propagation delay[2]	t_{pd2}	2900		7400	pS
Delay chip min delay[3]	$t_{delay-chip}$	1240		1765	pS
Input Data Buffer delay[4]	$t_{in-buffer}$	400		1450	pS
Input ClockBuffer delay[6]	$t_{in-buffer}$	360		710	pS
Clock Buffer delay[5]	$t_{clk-buffer}$	470		700	pS

Notes:
1. MC10E143.
2. SN10KHT5574.
3. MC10E196
4. MC10H115
5. MC10EL15
6. MC10EL57

As the clock buffer skew is negligible (~50pS), it is ignored. The input setup performance of the MC10E143 is always within the input performance of the SN10KHT5574.

Signal spread.

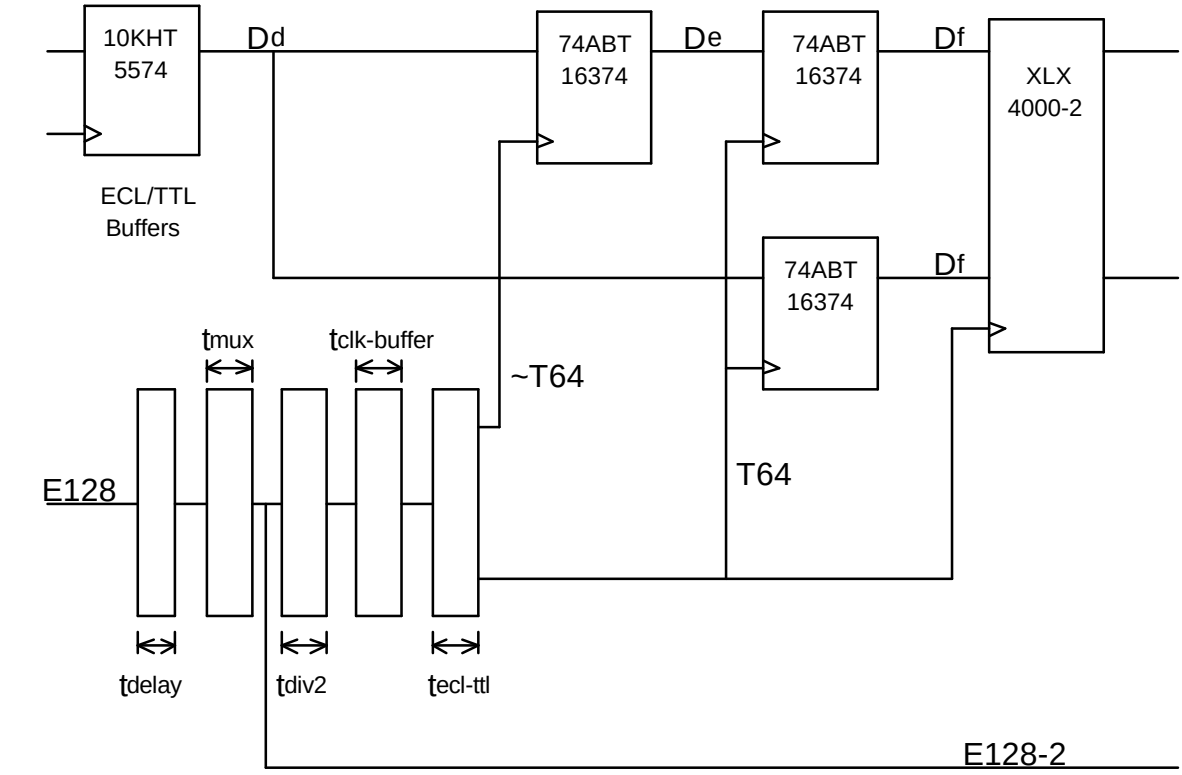
The following table indicated the amount of spread between the data signal and the clock signal. A negative value indicates clock lags data. As there needs to be at least 1000pS hold time (t_{holda}) and 1000pS setup time (t_{su2a}), for a clock period of 3906pS (256MHz) total delay must lie between -1000 and -2906pS.
Clock Error is the time difference of the clock signal and the data at the input to the board.
Clock P_d is the propagation delay of the clock circuit.
Data P_d is the propagation delay of the input buffers.
Rel Error is the relative error between the two at the appropriate data register inputs.
ΔT is the amount of extra delay inserted by the delay chip to meet the minimum setup time or hold time for the slowest register.

Clock Error	Clock P_d	Data P_d	Rel Error	ΔT	
-250	-2070	1450	-870	130	Fastest clock, slowest data
0	-2070	1450	-620	380	
250	-2070	1450	-370	630	
-250	-3175	400	-3025	1881[1]	Slowest clock, fastest data
-250	-1410	400	-1310	0[2]	
0	-3175	400	-2775	0	
250	-3175	400	-2525	0	
-250	-2070	400	-1920	0	Fastest clock, fastest data
0	-2070	400	-1670	0	
250	-2070	400	-1420	0	
-250	-3175	1450	-1975	0	Slowest clock, Slowest data
0	-3175	1450	-1725	0	
250	-3175	1450	-1475	0	

Notes:
1. Under these circumstances the hold time is violated; the clock must be delayed into the next data period. The threshold clock rate where delay need no longer apply is ~248MHz.
2. With Delay chip bypassed. With Delay Chip bypass selected the clock buffer chip inserts an additional 50pS.

These calculations use worst case propagation delays to calculate the extremes of time spread. If such component spread does occur, there is no one delay chip setting that will satisfy all conditions; it may be necessary to use components with similar or appropriate propagation delays.
Times used in this calculation were from the appropriate data books. These figures were based on test loads of 50pF. The actual loads will be around half this, so faster propagation times may affect various margins.

2.0 Second Stage.
This stage takes the 128MHz TTL data and broadens it out and slows it down to 64MHz. This uses a clock derived from the Master Clock signal.



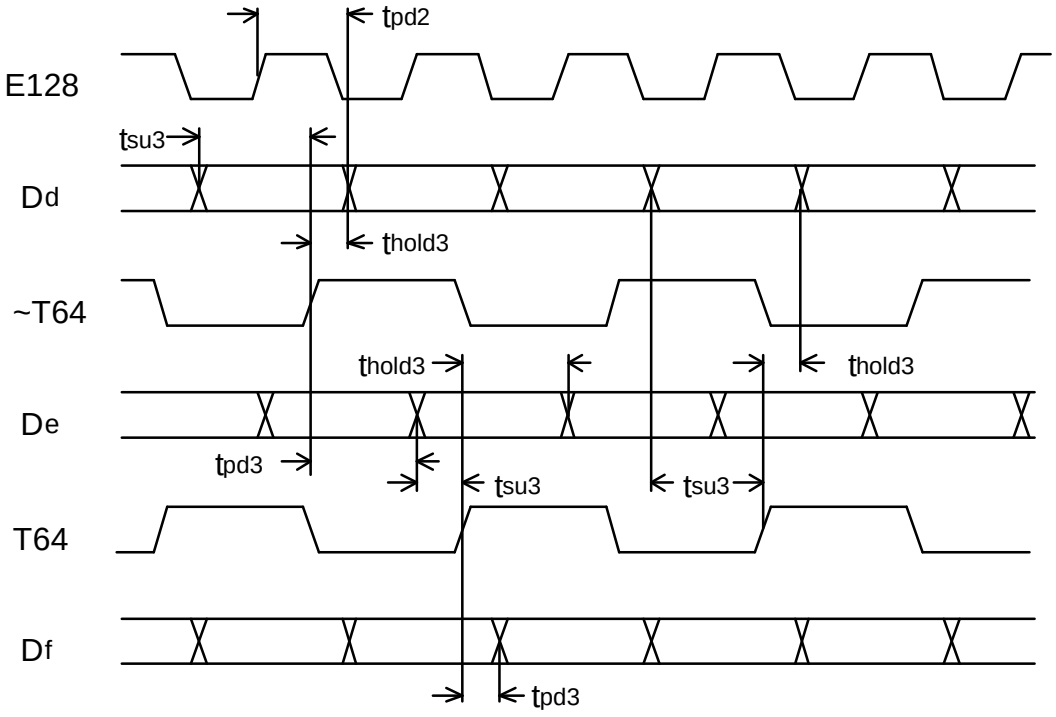


FIGURE A2
SECOND STAGE TIMING (TTL Clocks)

Name	Symbol	Min	Typ	Max	Units

Data Setup[1]	t_{su3}	1.1			nS
Data Setup[2]	t_{su3}	6.0			nS
Data Hold[1]	t_{hold3}	1.3			nS
Data Hold[2]	t_{hold3}	0			nS
Propagation delay[1]	t_{pd3}	2.7		5.9	nS
Propagation delay[2]	t_{pd3}			12.8	nS
Clock Divider delay[3]	$t_{clk\text{-}buffer}$	420	540	630	pS
Clock Buffer delay[4]	$t_{clk\text{-}buffer}$	1.7		4.1	nS

Notes:
1. 74ABT16374.
2. XC4013E-2, slew rate limited.
3. MC10EL32.
4. MC10ELT25.

Signal spread.

The following table indicated the amount of spread between the data signal and the clock signal. A negative value indicates clock lags data. As there needs to be at least 1300pS hold time (t_{holda}) and 1100pS setup time (t_{su2a}), for a clock period of 7812pS (128MHz) total delay must lie between -1100 and -6512pS.
Delay Chips is the number of delay chips cascaded together.
Clock P_d is the propagation delay of the clock circuit.
Data P_d is the propagation delay of the ECL to TLL registers/translators.
Rel Error is the relative error between the two at the appropriate data register inputs.
ΔT is the amount of extra delay inserted by the delay chip to meet the minimum setup time or hold time for the slowest register.

Delay Chips	Clock P_d	Data P_d	Rel Error	ΔT	
0	-2950	7400	4450	5550	Fastest clock, slowest data
1	-6330	7400	1070	2170	
2	-9710	7400	-2310	0	
0	-3610	2300	-1300	0	Slowest clock, fastest data
1	-5375	2300	-3075	0	

These calculations use worst case propagation delays to calculate the extremes of time spread. If such component spread does occur, there is no one delay chip setting that will satisfy all conditions; it may be necessary to use components with similar or appropriate propagation delays.
Times used in this calculation were from the appropriate data books. These figures were based on test loads of 50pF. The actual loads will be around half this, so faster propagation times may affect various margins.

Appendix B.

Bill Of Materials.

1.0 Buffer card.
1.1 Completed cards:

Project	Quantity	Comment
SEST	3	2 Working units + 1 Spare

Pulsar	2	Working + 1 Spare
Ateg	2	Test units/ backup spares

1.2 Other:

Project	Quantity	Comment
Prototype	2	1 or 2 to play with.

1.3 Parts List

Comment	Pattern	Qty	Components
10E143	PLCC28	4	U122 U123 U124 U125
10EL15	SOIC16	2	U109 U112
10EL57	SOIC16	1	U139
10ELT24	SOIC8	3	U106 U107 U108
10ELT25	SOIC8	17	U34 U35 U36 U37 U38 U39 U71 U72 U77 U78 U84 U87 U96 U97 U110 U111 U113
10H115PLCC	PLCC20	8	U140 U141 U142 U143 U144 U145 U146 U147
10H604	PLCC28	12	U116 U117 U118 U119 U120 U121 U128 U129 U130 U131 U132 U133
10HKT5574	SOIC24	8	U98 U99 U100 U101 U102 U103 U104 U105
26LS32	SOIC16	3	U136 U137 U138
26PIN	IDC26	2	J1 J2
74HCT157	SOIC16	1	U10
74ABT16245	SSOP48	1	U134
74ABT16374	SSOP48	14	U2 U3 U80 U81 U82 U83 U88 U89 U90 U91 U92 U93 U94 U95
74HC125	SOIC14	2	U135 U150
74HC1G00	SOT-535	2	U40 U151
74HC1G02	SOT-535	1	U41
74HC1G125	SOT-535	1	U152
74HC1G14	SOT-535	2	U11 U12
74HC1G32	SOT-535	1	U1
74LVT16374	SSOP48	32	U4 U5 U8 U9 U13 U14 U17 U18 U21 U22 U25 U26 U27 U28 U31 U32 U43 U44 U47 U48 U49 U50 U53 U54 U55 U56 U59 U60 U65 U66 U69 U70
BAV99LT1	SOT-23	6	D1 D2 D3 D4 D5 D6
CS-5210-1	TO-220	2	U19 U20
DS1820	PR35	3	U33 U42 U79
GVT71256G18T	TQFP100	16	U6 U7 U15 U16 U23 U24 U29 U30 U45 U46 U51 U52 U57 U58 U67 U68
LED	LED-555	17	LD1 LD2 LD3 LD4 LD5 LD6 LD7 LD8 LD9 LD10 LD11 LD12 LD13 LD14 LD15 LD16 LD17
LM3940B	TO-263B	2	U73 U114
NS93CS46P	DIP8	1	U148
VCX0_TTL_DUAL	DIP14	1	U126
XC1736P	DIP8	2	U127 U149
XC4010-PQ208	PQ208	3	U76 U85 U86
XC4013-208Q	PQ208	6	U61 U62 U63 U64 U74 U75
XC4013-PQ208	PQ208	1	U115
SW-SPST	TP11SH9ABE	2	SW1 SW2
R-2V	603	192	R86 R87 R88 R89 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R110 R111 R112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R126 R127 R128 R129 R130 R131 R132 R133 R134 R135 R136 R137 R138 R139 R140 R141 R142 R143 R144 R145 R146 R147 R148 R149 R150 R151 R152 R153 R154 R155 R156 R157 R158 R159 R163 R164 R165 R166 R167 R168 R169 R170 R171 R172 R173 R174 R175 R176 R177 R178 R179 R180 R181 R182 R183 R184 R185 R186 R187 R188 R189 R190 R191 R192 R193 R194 R195 R196 R197 R198 R199 R200 R201 R202 R203 R204 R205 R206 R207R208 R209 R210 R211

			R212 R213 R214 R215 R216 RT3 RT4 RT5 RT6 RT7 RT8 RT9 RT10 RT11 RT12 RT13 RT14 RT15 RT16 RT17 RT18 RT19RT20 RT21 RT22 RT23 RT24 RT25 RT26 RT27 RT28 RT29 RT30 RT31 RT32RT33 RT34 RT35 RT36 RT37 RT38 RT39 RT40 RT41 RT42 RT43 RT44 RT45RT46 RT47 RT48 RT49 RT50 RT51 RT52 RT53 RT54 RT55 RT56 RT57 RT58RT59 RT60 RT61 RT62 RT63 RT64 RT65 RT66
RES	603	61	R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R28 R29 R30 R31 R32 R33 R34 R35 R41 R42 R43 R44 R45 R49 R51 R52 R53 R162 R217 R218 R219 R236 R237 R238 R239 R240 R241 R242 R243 R244 R245 R246 R247 R248 R249 R250 R251 R252 R253 R255 R256 R257
RES103	603	15	R19 R24 R25 R26 R27 R37 R38 R40 R46 R47 R58 R232 R233 R234 R235
RES121	603	4	R220 R222 R228 R229
RES201	603	4	R221 R223 R230 R231
RES502	603	4	R224 R225 R226 R227
RES510	603	20	R20 R21 R22 R23 R36 R39 R48 R50 R54 R55 R56 R57 R59 R60 R61 R62 R63 R64 R65 R66
RT	603	32	RT71 RT72 RT73 RT74 RT75 RT76 RT77 RT78 RT79 RT80 RT81 RT82 RT83RT84 RT85 RT86 RT87 RT88 RT89 RT90 RT91 RT92 RT93 RT94 RT95 RT96RT97 RT98 RT99 RT100 RT101 RT102
RT/2	603	4	RT68 RT69 RT70 RT103
R_TO_-2V	603	19	R69 R70 R71 R72 R73 R74 R75 R76 R77 R78 R79 R80 R81 R82 R83 R84 RT1 RT2 RT67
R_TO_-5.2V	603	5	R67 R68 R85 R160 R161
LINK2X1	LK2X1M2	10	LK1 LK2 LK3 LK4 LK5 LK6 LK7 LK8 LK9 LK10
LINK2X2	LK2X2B	1	LK14
LINK3X1A	LK3X1	1	LK13
LINK3X1A	LK3X1M2	1	LK15
LINK4X1A	LK4X1	1	LK12
LINK8X1	LK8X1	1	LK11
D-C	603	458	C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C58 C59 C60 C61 C63 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C77 C78 C79 C80 C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99 C100 C101 C102 C103 C104 C105 C106 C107 C108 C109 C110 C113 C114 C115 C116 C117 C118 C119 C120 C121 C122 C123 C124 C125 C126 C127 C128 C129 C130 C131 C132 C133 C134 C135 C138 C141 C142 C143 C144 C145 C146 C147 C148 C149 C150 C151 C152 C153 C154 C155 C157 C159 C160 C161 C163 C164 C165 C166 C167 C168 C169 C170 C172 C173 C174 C175 C176 C177 C178 C179 C180 C181 C182 C183 C185 C186 C187 C188 C189 C190 C191 C192 C193 C194 C195 C196 C198 C199 C200 C201 C202 C203 C204 C205 C206 C207 C208 C209 C211 C212 C213 C214 C215 C216 C217 C218 C219 C220 C221 C222 C224 C225 C226 C227 C228 C229 C230 C231 C232 C233 C234 C235 C237 C238 C239 C240 C241 C242 C243 C244 C245 C246 C247 C248 C249C250 C251 C252 C253 C254 C255 C256 C257 C258 C259 C260 C261 C263 C264 C265 C266 C267 C268 C269 C270 C271 C272 C273 C274 C276 C277 C278 C279 C280 C282 C283 C284 C285 C286 C287 C288 C291 C292 C293 C294 C295 C297 C298 C299 C300 C301 C302 C304 C306 C307 C308 C309 C310 C311 C312 C313 C314 C315 C316 C317 C319 C321 C322 C323 C325 C326 C327 C328 C329 C330 C331 C332 C334 C335 C337 C338 C339 C340 C342 C343 C344 C345 C346 C347 C349 C350 C351 C352 C354 C355 C357 C358 C359 C360 C361 C362 C366 C367 C368 C370 C371 C372 C373 C374 C375 C376 C377 C378 C380 C381 C384 C385 C386 C387 C390 C391 C392 C393 C394 C395 C397 C398 C399 C400 C401 C402 C403 C404 C405

			C406 C407 C409 C411 C412 C413 C414 C416 C417 C420 C421 C422 C423 C424 C425 C427 C429 C430 C431 C432 C433 C434 C435 C436 C437 C438 C439 C441 C442 C443 C444 C445 C446 C447 C448 C449 C450 C451 C452 C454 C455 C456 C457 C458 C459 C460 C461 C462 C463 C464 C465 C467 C468 C469 C470 C471 C472 C473 C474 C475 C476 C477 C478 C480 C481 C482 C483 C484 C485 C486 C488 C489 C490 C491 C492 C498 C503
D-C	6032	28	C19 C57 C62 C64 C76 C111 C112 C136 C137 C158 C162 C289 C296 C303 C320 C341 C353 C356 C383 C388 C408 C415 C418 C419 C428 C497 C499
D-C	AXIAL1.0+	4	C504 C505 C506 C507
DC_S	603	13	C139 C140 C281 C324 C336 C363 C364 C369 C382 C389 C487 C494 C496
CAP	603	3	C500 C501 C502
CAP106	AXIAL0.2	1	C33
DIN41612	EURO160AM	2	JA1 JA2
TESTPOINT	TESTPOINT	112	PP1 PP2 PP3 PP4 PP5 PP6 PP7 PP8 PP9 PP10 PP11 PP12 PP13 PP14 PP15 PP16 PP17 PP18 PP19 PP20 PP21 PP22 PP23 PP24 PP25 PP26 PP27 TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP28 TP29 TP30 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38 TP39 TP41 TP42 TP43 TP44 TP45 TP46 TP47 TP48 TP49 TP50 TP51 TP52 TP53TP54 TP55 TP56 TP57 TP58 TP59 TP60 TP61 TP62 TP63 TP64 TP65 TP67 TP68 TP69 TP70 TP71 TP72 TP73 TP74 TP75 TP76 TP77 TP78 TP80 TP81 TP82 TP83 TP84 TP85
GND	TESTPOINT	40	PP28 PP29 PP30 PP31 PP32 PP33 PP34 PP35 PP36 PP37 PP38 PP39 PP40 PP41 PP42 PP43 PP44 PP45 PP46 PP47 PP48 PP49 PP50 PP51 PP52 PP53 PP54 PP55 PP56 PP57 PP58 PP59 PP60 PP61 PP62 PP63 PP64 PP65 PP66 PP67

2.0 Buffer Backplane.

2.1 Completed cards:

Project	Quantity	Comment
SEST	1	1 Bin
Pulsar	1	1 Bin
Ateg	2	2 Bin

2.2 Other:

Project	Quantity	Comment
Prototype	1	

2.3 Parts List

Part	Quantity

Questions/Notes.

4.0 Miscellaneous.

4.1 Data Buffer Card V1.0 faults and missing features.

4.1.1 Data Buffer Card V1.0.

- ✔ "Lamp Test" signal wrong sense. Move the Master Done single gate driver to before the quad 2:1 mux.
- ✔ More Event Generator lines to the MCC Xilinx.
- ✔ BCC ~WR and ~STRB to the MCC Xilinx.
- ✔ Schottky snuffer diodes back to front.
- ✔ Need for parallel resistors in 3.3V regulators.
- ✔ Larger footprints for single gate devices (SOT-535?).

Large holes for wirewrap wires for unexpected modifications.
#ADSC on memory ICs should connect to GND.
Missing 64MHz clock signal to MCC Xilinx.
Test points for DONE pins.
Lengthen pads on 100 pin QFP's (or move them out a bit).
Tie unused pins on U150 (74x125 BLANK driver) to driven source.
Nets B1_A_D47 and B0_A_D47 on pins 5 and 6 respectively on U80 need to be swapped.
*More control lines from MCC to INPUT Xilinx and possibly DEMUX Xilinx.
One or more large tantalum capacitors on 3.3V rails.
Check timing of clock signals to 'input' Xilinx and '374s downstream. (reverse order of delivery of balanced ECL signal to 10ELT25's?)
More signal testpoints using vias.
Need to disable "output enable" signals on the 74LVT1637s that drive the signals to "DEMUX" until "DEMUX" has been configured.
Labels on LEDs - Xilinx Done's.
Lengthen 128MHz signal to MUX Xilinx by ~1nS.
Feed MCC Xilinx with 128MHz signal (p162?) and drive ELT24 chip (p163?) for divided clock. Add an ECL mux to 128MHz signal feeding backplane drivers for lower clock rates.
Run signal from MUX Xilinx to ALIGN Xilinx to disable ALIGN's output if MUX Xilinx not configured.
Run signal from ALIGN Xilinx to DEMUX Xilinx to disable DEMUX's output if ALIGN Xilinx not configured.
Run signal from DEMUX Xilinx to MCC Xilinx to disable MCC's outputs to 74LVT16374 output enable pins if DEMUX Xilinx not configured. Use jumper to option permanent enable.
Run signal from INPUT Xilinx to 74ABT16374's output enable pins disable these if INPUT Xilinx not configured. Use jumper to option permanent enable.
Fix problem of asynchronous Noise Cal switching signal.
Fix problem of -WAIT line being pulled down when board power off.

4.1.2 Data Buffer Card Clock Generator.
Missing links to 'SELx' pins on U5.
Link LK5 needs to be 2mm.

4.2 Data Buffer Motherboard V1.0 faults and missing features.

Need to move event generator connector lower (ie further away from BCC IF connector) by around 300mil.

No connection for some decouple caps.

Need some large decoupling capacitors.

4.3 Correlator Accumulator Card V1.0 faults and missing features.

PCB not right size (short?).

Swap signals ~BCC_WAIT and ~BCC_REQ going to backplane connector.

Place default links on LK6, LK7 and LK8.

Schottky snuffer diodes back to front.

Need for parallel resistors in 3.3V regulators.

Larger footprints for single gate devices (SOT-535?). Investigate using quad packs at some locations.

Wire wrap wire holes for unexpected modifications.

Interference between U85 and lower EURO connector mounting tab.

Test points for DONE pins.

Mounting holes for regulators need to be > 3mm dia.

Connections pin holes for regulators need to be bigger.

Disconnect the "Master Reset" pin from GND on all the 10H604 data output drivers.

One or more large tantalum capacitors on 3.3V rails.

More signal testpoints using vias.

TQ2018 foot print needs modification.

Buffer_blank_0 needs (optional) termination on board.

-DMA_TALK needs to connect to pin 109 on BCC Xilinx.

Fix problem of -WAIT line being pulled down when board power off.

4.4. Correlator Accumulator Motherboard faults and missing features.

Poor labelling around EG 34 way connector, 26 way BCCIF connector and the 2 X 40 way DMA connectors.

All buffer_blank_x (excluding buffer_blank_0) needs (optional) termination on board.

A set of terminals that connect into the 2 interrupt lines in the DMA bus.

4.5. Greenbank Correlator Card Production modifications.

To meet the requirements for the wideband correlator, some modifications need to be performed to the Greenbank Correlator Card. These modifications are all non-destructive and can be easily reversed if required.

1. Remove R1 and R2.
2. Remove C1 and replace with a wire link.
3. Remove all wire links at sites 4A and 6A.
4. Remove SIP resistor packs at sites 2AL, 3AL, 7AL, and 8AL.
5. On underside of board, using wirewrap wire, connect one wire in the following sequence: 4A-3, 5A-3, 4A-5.
6. On underside of board, using wirewrap wire, connect one wire in the following sequence: 6A-3, 5A-4, 6A-5.
7. On underside of board, using wirewrap wire, connect a wire between the following pins on 2D, 4D, 6D and 8D: pin 8 - pin 40, pin 10 - pin 36, pin 21 - pin 67, pin 20 - pin 68.

%% END %%